I. M. Dharmadasa

Advances in THIN-FILM SOLAR CELLS

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Preface

Sunlight was first converted into electricity by Edmund Becquerel in 1839, but until the 1950s, no considerable development had taken place. However, during the two decades of the 1950s and the 1960s, Si-based solar cells were developed, manufactured, and used in applications such as satellites and remote communication stations. The first oil crisis, in the early 1970s, gave a huge push to the search for alternative energy conversion methods, and researchers actively searched for new materials and low-cost device structures. As a result, thin-film solar cells based on III-V compounds (GaAs and InP), amorphous Si, CdTe, and $CuInGaSe_2$ (CIGS) were introduced to mainstream solar energy conversion. In the early 1990s, dye-sensitised solar cells were introduced, and organic solar cells came in the early 2000s. With the renewed interest in nanomaterials, researchers worldwide are exploring the ways of using new materials in solar cell devices. At present, all these photovoltaic (PV) fronts are moving toward producing low-cost and high-efficiency solar cells to convert sunlight into electricity.

The main hurdle in the rapid market penetration of solar energy applications is their high cost. Although there are active research programmes to reduce manufacturing costs and increase conversion efficiencies, the progress is painfully slow for various reasons—one reason being the lack of deeper understanding of material issues and physics behind solar cell devices. This book does not deal with well-documented semiconductor properties and device principles but presents the latest developments and advances in thin-film solar cells, with an introduction to the most required background knowledge. The targeted audience will be undergraduate and postgraduate students in science and engineering; electronic device

researchers in chemistry, material science, physics, mathematics, and engineering; and PV module developers and technologists in the industry. This book concentrates mainly on advances in thin-film solar cells based on CdTe-, CIGS-, and GaAs-based devices, but the ideas are equally applicable to all thin-film solar cells.

Chapter 1 of this book introduces solar energy conversion to all readers in a simple manner with the aid of diagrams, references, and animations placed on the author's website. The next chapter provides a brief status report on PV technology. The main barrier in the PV sector is the high manufacturing cost due to the use of expensive materials (Si and III-V compounds) and the high energy consumption during materials growth and device processing. The initial high capital cost of equipment also exacerbates this situation. As a solution to this, a low-cost and scalable materials growth technique (electro-chemical deposition) for II-VI and alloy compounds will be described in chapter 3. This growth method is also a suitable low-cost technique for growing nanomaterials for various other applications in nanotechnology. In all solar cells, two electrical contacts are needed to extract the photo-generated charge carriers from the device and, hence, these metal/semiconductor (MS) interfaces play a very important role in the overall performance. Chapter 4 summarises the most striking recent breakthroughs which improved the understanding of PV action in thin-film solar cells. This chapter describes the history of the CdTe solar cell, the application of new ideas to this device, the formation of a new concept to describe the solar energy conversion process, and the way forward for the development of the device. Chapter 5 extends the applicability of the Fermi-level pinning concept to CIGS-based solar cells. The next three chapters are devoted to revisiting the current practice in tandem solar cells based on tunnel junctions and the use of multi-layer graded bandgap device structures in solar energy conversion. The latter device design has been experimentally tested with a well-researched GaAs/AlGaAs system. This device has shown highest reported open circuit voltage of 1175 mV with the highest achievable fill factor of ~0.86 for a single device. The new device concept is mainly based on a set of defects within these devices, and chapter 9 describes the effects of defects on the performance of solar cells. It also describes

the way forward for dealing with defects in order to achieve higher performance in devices. Chapter 10 is for the general public and describes the scenario of a future dominated by solar energy. This is based on author's two decades of public understanding of science activities and real projects carried out on the ground. The solar village project designed and piloted successfully by the author is described, and the replication plans are indicated in this chapter. There are two short chapters included at the end of this book—chapter 11 presents the evidence collated to date for Fermi-level pinning in GaAs-based solar cells, and chapter 12 indicates some thoughts on future directions of thin-film solar cell research.

I am grateful to all the people who have supported me to develop and progress in this sector. My PhD supervisors, late Sir Professor Gareth Roberts and Professor Mike Petty at Durham University, put me on the right track at the very beginning, in the late 1970s. Working with active scientists in the field, Professors R. H. Williams and E. H. Rhoderick, enabled me to be well established in this field during my four-year postdoctoral research in University College Cardiff, in early 1980s. Since then, I have worked on and learned the subject from numerous colleagues from chemistry, physics, mathematics, and engineering disciplines, both in academia and in the industry (BP Research, Sunbury). During the last two decades of my academic career at Sheffield Hallam University, many postdoctoral researchers, 14 PhD students, and numerous visiting researchers contributed to this work in order to understand the chemistry and physics behind these complex materials and devices. University lecturing on relevant subjects like electricity and magnetism, thermodynamics, solid-state physics, quantum mechanics, high-specification materials, device design and manufacture, and Si processing in clean room environment for over three decades helped me in understanding these complex devices. This accumulated knowledge, new breakthroughs, and recent advances are presented in this book to share with the present and future scientists, engineers, and the general public. I am grateful to my immediate family for their help and support during this journey. In particular, I thank Dahiru Diso, Osama Elsherif, Ajith Weerasinghe, Obi Kingsley Echendu, Fijay Bin Fauzi, Tamara Dharmadasa, Ruvini Dharmadasa, and Asela Dharmadasa for their

contributions during the preparation of this book. I also thank Sidath Kalyanaratne and Nishith Patel for preparing some of the diagrams used in this book.

Finally, this book is dedicated to my beloved parents, who worked hard to support me during my childhood with limited resources while living in a sun-rich environment in Sri Lanka. I am hopeful that this book will contribute to reverse this situation for future generations by bringing prosperity to all the people who live wherever the sun is shining.

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March 2012

List of Symbols and Abbreviations Used in the Book

h	Planck constant
f	frequency in Hz
e	electronic charge
k	Boltzmann constant
χ	electron affinity
ε_0	dielectric permittivity of free space
ε_s	dielectric permittivity of semiconductor
ε_r	relative permittivity of semiconductor
σ	electrical conductivity
T	temperature in Kelvin
ϕ_b	potential barrier height
ϕ_m	metal work function
E_g	energy bandgap of a semiconductor
A^*	Richardson constant for thermionic emission
S	area of a solar cell
n	ideality factor of a diode
V_{oc}	open circuit voltage of solar cells
I_{sc}	short circuit current of solar cells
J_{sc}	short circuit current density of solar cells
FF	fill factor, or curve factor, of solar cells
η	solar to electric power conversion efficiency
CdTe	cadmium telluride
CIGS	copper indium gallium diselenide
GaAs	gallium arsenide
AlAs	aluminium arsenide

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Chapter 1

Photovoltaic Solar Energy Conversion

1.1 Introduction

Sunlight consists of electromagnetic radiation in the regions of ultraviolet (UV), visible light, and infrared (IR) radiation. The solar spectrum reaching the earth's surface undergoes various absorptions in the air atmosphere, and the average solar energy falling on the earth's surface is generally known as air-mass 1.5 (AM1.5) irradiation, which is equal to approximately 100 $mWcm^{-2}$. This quantity is equal to $\sim$1.0 kW of power falling on every square metre, which humankind has not yet effectively utilised. The shape of the solar spectrum and the absorption of various wavelengths under AM1.5 conditions are shown in Fig. 1.1. Traditionally, there are two ways of capturing solar energy. One method is to absorb mainly the heat energy (or IR radiation), and this is generally known as 'solar thermal technology'. The second method is to convert UV and visible light (photons) directly into electricity (measured in volts). Since the photons are directly converted into volts, this method is known as 'photovoltaic conversion' (PV conversion for short). This book concentrates only on the second method, which is PV conversion.

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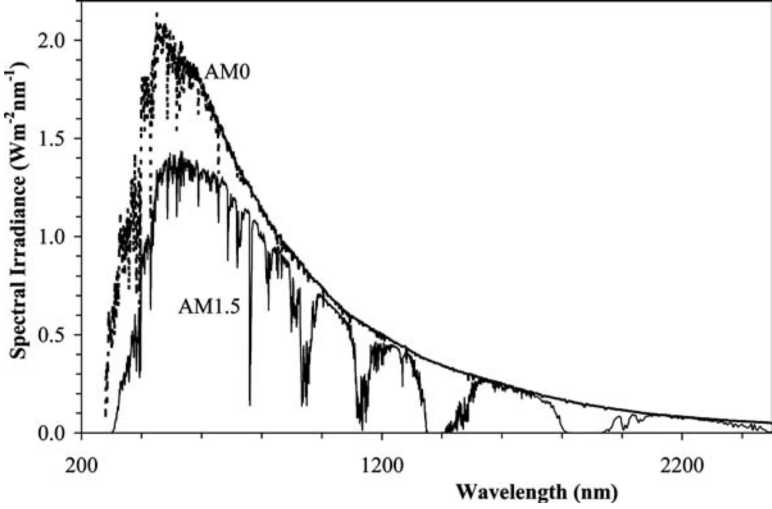

Figure 1.1 The approximate shape of the solar spectrum under AM1.5 condition. The shape of the spectrum before entering the air atmosphere (AM0 condition) is also shown for comparison [1].

1.2 Photovoltaic Effect

In the process of effective PV energy conversion, four basic steps must be brought together simultaneously. These are:

(a) Absorption of photons using a suitable material
(b) Creation of charge carriers (electron-hole, or e-h pairs) mainly by breaking bonds between atoms
(c) Separation of oppositely charged free carriers before their recombination
(d) Collection or transportation of photo-generated charge carriers through electrical contacts and their passage through an external circuit to create useful electric current.

If any of these four processes is hindered or not taking place, the device will show poor conversion efficiency, or zero PV activity. Bringing these four stages together by selecting the right materials and putting them together in a suitable device structure is a challenging task. In PV research, this task is twofold — (i) exploring

new materials with the right properties to absorb light and create charge carriers effectively and (ii) fabricating suitable devices to separate and transport charge carriers out of the device and through an external circuit.

1.3 Solar Energy Materials

All materials around us can be classified into three main groups: electrical conductors, semiconductors, and insulators. This classification can be done according to the electrical conductivity (σ) or the energy bandgap (E_g) of the materials. Table 1.1 summarises the two main properties of these different classes of materials, but it should be noted that there is no clear demarcation among these classes. For more details and specific properties of different materials, the reader is requested to refer to already published books in materials [2–4], solid-state physics [5–7], and solid-state chemistry [8–9].

The materials used for the absorption of light and creation of charge carriers come from semiconductor families. Over the past 70 years, scientists have identified many different semiconducting materials with a wide variety of properties. Table 1.2 displays some relevant elements from the Periodic Table, and Table 1.3 shows many different semiconductors available today. The task for the PV community is to identify the most suitable semiconductors to effectively absorb light and create charge carriers for solar energy conversion. High optical absorption, a direct instead of indirect bandgap, and low density of recombination centres, together with required mechanical strengths and stability, are some of the desired properties for solar energy materials. In addition, these materials should have the required qualities to make appropriate electronic devices in order to separate and collect photo-generated charge carriers. When these materials are prepared in the form of thin films

Table 1.1 A summary of two main properties of different classes of electronic materials

Parameter	Electrical Conductors	Semiconductors	Electrical Insulators
σ $(\Omega\,\mathrm{cm})^{-1} \equiv \mathrm{S}$	$\sim 10^{8}$–10^{1}	$\sim 10^{1}$–10^{-8}	$\sim 10^{-8}$–10^{-20}
E_g (eV)	$\sim$ 0.3 or negative values	$\sim$ 0.3–4.0	$\sim$ 4.0–10.0

with thicknesses of a few microns, the situation becomes even more complex due to the effects of surface states.

Table 1.2 The most common elements used for the production of semiconductors, with their groups assigned in the Periodic Table

Group I	Group II	Group III	Group IV	Group V	Group VI
Cu	Zn	B	C	N	S
Ag	Cd	Al	Si	P	Se
		Ga	Ge	As	Te
		In	Sn	Sb	O

Table 1.3 A summary of semiconductor material families available for use in PV devices

Semiconductor Family	Examples of Semiconductors
Elemental semiconductors	C, Si, Ge
III–V semiconductors	AlN, AlP, AlAs, AlSb
	GaN, GaP, GaAs, GaSb
	InN, InP, InAs, InSb
II–VI semiconductors	ZnS, ZnSe, ZnTe, ZnO
	CdS, CdSe, CdTe, CdO
Ternary compound semiconductors	$CuInSe_2$ (CIS), $Cd_xMn_{(1-x)}Te$,
	$Cd_xHg_{(1-x)}Te$, $Al_xGa_{(1-x)}As$
Quaternary compound semiconductors	$CuInGaSe_2$ (CIGS), AgInGaSSe, CuZnSnSSe

1.4 Electronic Devices Used for Solar Energy Conversion

Once the suitable solar energy materials are selected, the optimum growth conditions have been established, and the materials are fully characterised for their mechanical, structural, optical and electrical properties, the next task is to design and fabricate an effective electronic device capable of creating and separating photo-generated charge carriers before they recombine. This requires a strong built-in electric field within the electronic device. The heart of a PV device is, therefore, one or more interfaces created by combining suitable semiconductors and two electrical contacts to extract charge carriers from these devices. Therefore, in a typical PV device, several interfaces can be incorporated, made out of

electrical conductors, semiconductors, and insulators. The following sections examine different basic interfaces used in electronic device structures. Several of these basic interfaces can then be combined to form an efficient PV solar cell.

1.4.1 *p-n Junctions*

The most basic interface is the p-n junction formed within one semiconductor crystal lattice having p-type and n-type electrical conduction in two adjacent regions. These types of junctions are generally known as homo-junctions, and the energy band diagram is shown in Fig. 1.2. The slope produced in the energy band diagram represents the built-in electric field ($E = -\mathrm{d}V/\mathrm{d}X$) available within the device. The region here with this band bending (or the area with the built-in electric field) is known as the 'depletion region', and this region is the heart of this basic electronic device. The basic properties of p-type and n-type semiconductors are summarised in Table 1.4 for quick reference, but readers are advised to refer to a suitable textbook for further information on fundamental materials and device properties [10–12].

When photons with energy (hf) greater than the bandgap of the semiconductor ($hf \geq E_\mathrm{g}$) fall in the depletion region, photons are absorbed and bonds between the atoms are broken to create free e-h pairs. The existing internal electric field separates these photo-generated charge carriers due to their opposite charges,

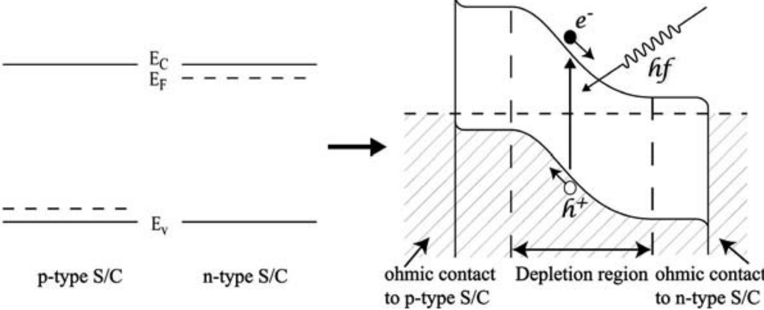

Figure 1.2 The energy band diagram of a p-n homo-junction and the mechanism of PV activity within a solar cell based on a p-n junction.

Table 1.4 A summary of main properties of p-type and n-type semiconductors

p-Type Semiconductors	n-Type Semiconductors
• The majority charge carriers are holes. • The minority charge carriers are electrons. • These semiconductors are doped with externally added acceptors, native defects, or variation in composition. • The Fermi level is positioned close to the valence band.	• The majority charge carriers are electrons. • The minority charge carriers are holes. • These semiconductors are doped with externally added donors, native defects, or variation in composition. • The Fermi level is positioned close to the conduction band.

forcing them in opposite directions, towards the two electrical contacts on both sides of the junction. If the built-in electric field is weak or non-existent, photo-generated charge carriers will recombine again and the photo-current will be low or zero. Therefore, the key to improving the PV activity is to fabricate a healthy depletion region, with a strong built-in electric field, using a semiconductor with high optical absorption properties and low recombination centres.

The action of a solar cell based on a p-n junction is demonstrated by animation on Dharme's blog at: www.apsl.org.uk to help beginners in this field visualise the PV process.

1.4.2 *p-i-n Junctions*

The production of a healthy depletion region depends on the doping concentration of the two semiconductor regions used to fabricate the p-n junction. Low doping concentrations produce a wide depletion region, and heavy doping concentrations create a thin depletion layer, which are not helpful for PV conversion. Optimising the doping concentration to create a depletion region width comparable to the thickness of a thin film solar cell, typically in the order of 2 μm, to achieve the best performance is a real challenge faced by material scientists and device physicists during the research and development phase. The exact value of the depletion region width depends on the device design planned for a particular purpose.

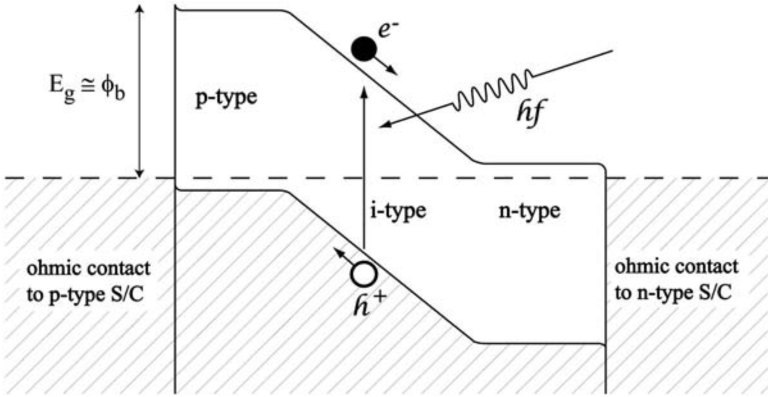

Figure 1.3 The energy band diagram of a p-i-n diode and the mechanisms of PV activity within the device.

One improvement generally used is the fabrication of p-i-n-type interfaces. The energy band diagram of a p-i-n device is shown in Fig. 1.3, and an intrinsic (or insulating) semiconductor is sandwiched between p- and n-type semiconducting layers.

This arrangement aligns the Fermi levels of the two semiconductors through the intrinsic layer to create a strong internal electric field throughout the i-layer and hence control the width of the depletion region for a specific application. This is also a reliable method to form a high potential barrier approaching the bandgap of the semiconducting material used ($E_g \approx \phi_b$). Animation to illustrate the formation and use of a p-i-n diode as a solar cell is presented in Dharme's blog at www.apsl.org.uk. This will be helpful in understanding electron transfer during junction formation, band-bending process, and visualisation of the PV actions of the p-i-n-type solar cell device.

1.4.3 *Hetero-Junctions*

A hetero-junction is another simple modification of the p-n-type interface. Instead of one semiconducting material on both sides of a homo-junction, two different semiconductors are used to form the interface (Fig. 1.4). The main difference is the existence of two different energy bandgaps on either side. An advantage of

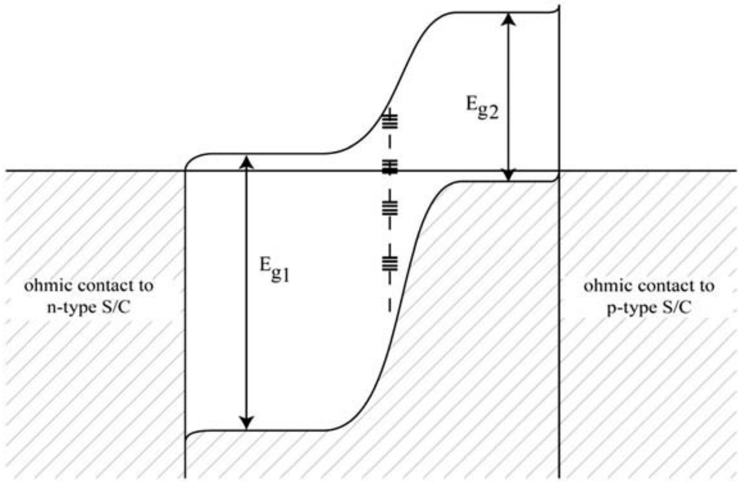

Figure 1.4 The energy band diagram of a hetero-junction diode with two ohmic contacts on both sides. Energy bandgaps on two sides are different, and interface states have been introduced.

using two different semiconductors in the device is the absorption of different regions of the solar spectrum. However, in hetero-junctions, one semiconductor needs to be physically grown on another semiconductor, which can introduce detrimental surface states (or defects) affecting the performance of the device due to crystal lattice mismatch, the existence of surface states, and foreign atoms such as carbon and oxygen.

1.4.4 *n-n and p-p Junctions*

Interfaces with internal electric fields can also be created using only one type of semiconductor, by combining materials having different energy bandgaps as shown in Fig. 1.5. Although the potential step created at each interface is small in this case, these can be joined together to form graded bandgap multi-layer solar cells, as described in detail in section 1.6 and later in this book.

1.4.5 *Metal/Semiconductor (or Schottky) Contacts*

A solar cell device with one or more interfaces creating its depletion region, and hence the built-in electric field, requires

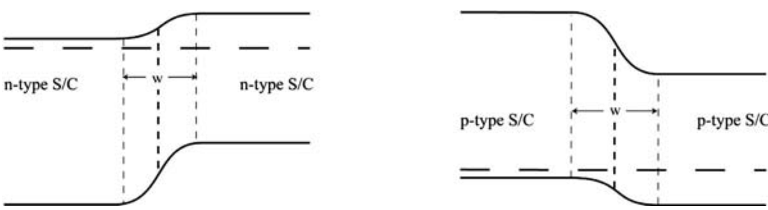

Figure 1.5 Hetero-junction interfaces from n-n and p-p junctions creating small steps of potential barriers.

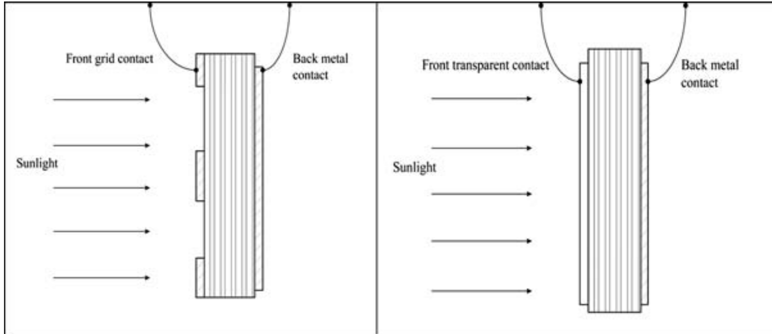

Figure 1.6 Solar cells based on a grid type or transparent front contact providing the conditions required for PV solar cells.

two electrical contacts on either side to effectively collect the photo-generated charge carriers and transport them through an external circuit. These electrical contacts are usually formed using metal/semiconductor (MS), or Schottky, contacts. The front electrical contact should either take the form of a grid contact to minimise the effect of shading or be transparent to incoming light (Fig. 1.6). Depending on the design of the solar cell device, the MS interface could have either ohmic or rectifying properties. For comprehensive information on MS interfaces, readers can refer to textbooks written on this particular subject [13, 14].

As a brief summary of Schottky barrier formation, Fig. 1.7 presents the energy band diagram of a metal/n-type semiconductor interface. When a metal having a work function ϕ_m is brought into intimate contact with an n-type semiconductor having an electron affinity χ, a potential barrier height (ϕ_b) is formed at the interface. If there are no surface states or other defects arising from the material,

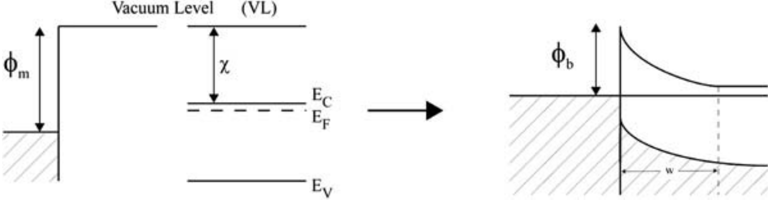

Figure 1.7 Schottky barrier formation at a metal/n-type semiconductor when an ideal interface is formed between the two materials.

the ϕ_b formed at this interface is given by:

$$\phi_b = \phi_m - \chi \tag{1.1}$$

The formation of potential barriers at the metal/p-type semiconductor is very similar, but the band bending will be in the opposite direction, forming potential barriers for the flow of holes. The above description is valid only for ideal interfaces, but the situation is very different for interfaces strongly affected by semiconductor defects, surface or interface states. In these situations, the Fermi level will be pinned by the defect states and hence ϕ_b is independent of the metal used for the formation of the electrical contact. The drastic effects of Fermi-level pinning will be discussed in detail in later chapters of this book.

The nature of the potential barrier formed at the MS interface will govern the electrical properties of this interface. If the ϕ_b is in excess of ~0.40 eV and the width of the depletion region (W) is considerable, the interface will have rectifying electrical properties described by Eq. 1.2 [13, 14].

$$I_D = SA^*T^2 \cdot \exp\left(\frac{-e\phi_b}{kT}\right)\left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \tag{1.2}$$

where I_D = Electric current in dark condition
S = Area of the contact
A^* = Richardson constant for thermionic emission
T = Temperature in Kelvin

$e =$ Electronic charge
$\phi_b =$ Potential barrier height
$k =$ Boltzmann constant
$n =$ Ideality factor of the diode

These types of potential barriers are formed when the semiconductor has moderate doping concentration of $\sim 10^{15}$–10^{17} cm^{-3}. When the ϕ_b is less than $\sim$0.40 eV — or the depletion region is narrow — the electrical conduction through the interface will exhibit linear (ohmic) behaviour due to the ease of electron transfer in both directions. Heavy doping, in excess of 10^{18} cm^{-3}, will form a thin enough depletion layer, enabling charge carriers to tunnel through the interface showing ohmic behaviour. Both rectifying and ohmic electrical contacts can be incorporated in PV solar cells in order to maximise the internal electric field present in these devices.

1.4.6 *Metal-Insulator–Semiconductor Interfaces*

In general, the ϕ_b values obtained at MS interfaces are much smaller than those of p-n junctions for a given semiconductor. As indicated in Fig. 1.8, the Schottky barrier represents approximately half of a p-n junction and, hence, a lower ϕ_b.

This disadvantage can be removed by incorporating an insulating layer, as shown in Fig. 1.9. The suitably thin insulating layer decouples the metal from the semiconductor and increases the band bending or the potential barrier at the interface. The rectification property of this structure improves, and the interface behaviour is described by Eq. 1.3 [15]:

$$I_D = SA^*T^2 \exp(-\chi^{1/2}\delta) \exp\left(\frac{-\phi_b}{kT}\right) \exp\left(\frac{eV}{nkT}\right) \tag{1.3}$$

where χ, in electron volts, is the mean barrier height presented by the interfacial layer of thickness, δ, in Angströms (Å).

As described in section 1.5.3, the open circuit voltage (V_{oc}) of a solar cell is a function of the ϕ_b and, therefore, this is a method used to enhance the V_{oc} of PV solar cells based on Schottky diodes. The insulating layer brings an additional advantage of minimising the interactions between the metal and the semiconductor. In the case

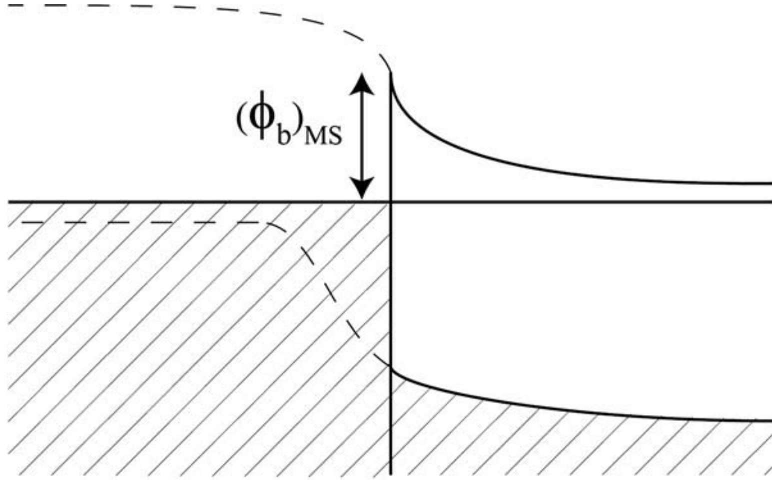

Figure 1.8 A schematic diagram showing that a Schottky barrier is only a half of a p-n junction in the case of an ideal interface.

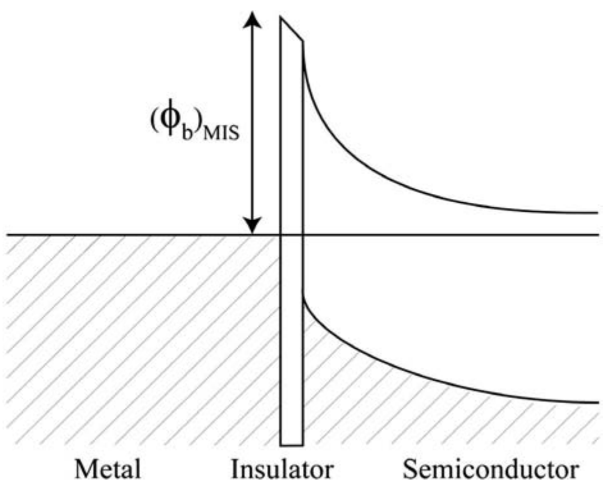

Figure 1.9 The enhancement of the ϕ_b and the decoupling of two materials by the incorporation of an insulating layer at the interface.

of an organic insulator, this layer prevents the in- and out-diffusion of metal and semiconductor elements. This layer also prevents chemical reactions between the two inorganic materials, the metal and the semiconductor. This leads to an increase in the device lifetime, removing ageing effects at the electrical contact. This is an ideal way to improve performance, stability, and lifetime of PV solar cells by fabricating hybrid-devices combining inorganic and organic materials.

In the place of an insulating layer, a p-type conducting polymer can be used. In this case, the intermediate layer can have large thicknesses, which will be an advantage in producing organic-inorganic hybrid devices.

1.5 Characteristics of a Solar Cell

As described in the above sections, a typical PV cell contains one or more interfaces producing rectifying property and two electrical contacts on both sides to collect charge carriers. The nature of the two electrical contacts can vary according to the device design used, with generally used ohmic contacts. However, metal contacts with rectifying properties can also be used to enhance the existing electric field within the device, as described in later chapters of this book. The following section uses a simple solar cell device structure based on a rectifying Schottky diode to illustrate the characteristics of a solar cell and its conversion efficiency. Details of other PV solar cell devices are well documented in previous publications [16–20].

1.5.1 *I-V Characteristics of a Solar Cell Under Dark Conditions*

Figure 1.10 shows a schematic diagram and the corresponding energy band diagram of a simple solar cell based on a rectifying Schottky contact formed on an n-type semiconductor. The front contact can be fabricated using a transparent electrical contact or grid type contact to minimise the effect of shading. The back electrical contact is a usual ohmic contact to collect charge carriers.

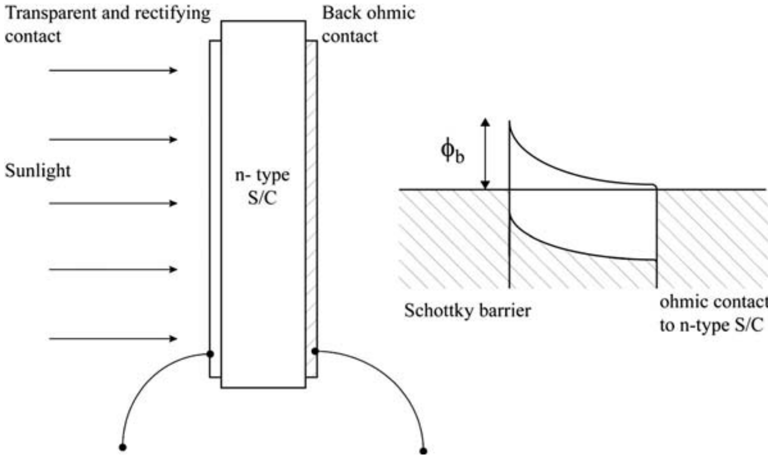

Figure 1.10 A schematic diagram of a PV solar cell based on a rectifying Schottky contact and an ohmic back contact formed on an n-type semiconductor, together with its energy band diagram.

The current-voltage (I-V) characteristics of a Schottky diode under dark conditions can be expressed by Eq. 1.2 [13, 14]:

$$I_{\mathrm{D}} = SA^{*}T^{2} \cdot \exp\left(\frac{-e\phi_{\mathrm{b}}}{kT}\right)\left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \tag{1.2}$$

or

$$I_{\mathrm{D}} = I_{0}\left[\exp\left(\frac{eV}{nkT}\right) - 1\right] \tag{1.4}$$

where I_0 represents the saturation current.

For externally applied voltages across the diode above ~75 mV ($V \geq 75$ mV):

$$\exp\left(\frac{eV}{nkT}\right) \gg 1 \tag{1.5}$$

Therefore, Eq. 1.4 can be simplified to the following form:

$$I_{\mathrm{D}} = I_{0} \cdot \exp\left(\frac{eV}{nkT}\right) \tag{1.6}$$

The rearrangement of this equation provides a useful relation to analyse the I-V data measured under dark conditions for a PV device.

$$\log_{10}(I) = \left(\frac{e}{2.303nkT}\right) \cdot V + \log_{10}(I_{\mathrm{D}}) \tag{1.7}$$

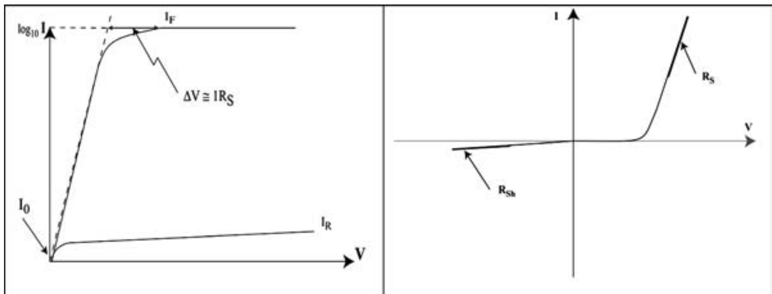

Figure 1.11 The log-linear and linear-linear graphs plotted for detailed analysis of dark I-V characteristics of PV solar devices.

A plot of $\log_{10}(I_D)$ versus the voltage applied (V) across the device takes the form of Fig. 1.11 for a practical device. It should be noted that both forward and reverse currents are plotted here in the same quadrant by changing the sign of the reverse voltages for convenience.

The rectification factor (RF) of the device, as defined by the expression RF = forward current/reverse current at a given voltage (say at $V = 1.0$ V) is a good indicator of the quality of rectifying diode. For an efficient solar cell, a large RF is desirable although an RF with a value of approximately 10^3 is sufficient.

The straight-line portion of the graph provides a value for the n from its gradient:

$$\text{Gradient} = \left(\frac{e}{2.303nkT}\right) \tag{1.8}$$

This is a useful parameter as it provides a general idea about the current transport through the potential barrier [13]. For an ideal diode, the current transport takes place only through thermionic emission over the potential barrier and, hence, the n is equal to unity ($n = 1.00$). If the depletion region and the interface are full of recombination and generation (R&G) centres, the current transport is dominated by the R&G process and the value of the n becomes 2.00. In practical devices, both these transport mechanisms take place in parallel and, therefore, n takes values between 1.00 and 2.00. The situation becomes even more complicated when there is a large series resistance (R_s) present in the device structure. The

value of R_s can be approximately evaluated using the potential drop at the high forward end of the I-V curve using Eq. 1.9:

$$\Delta V = I \cdot R_s \tag{1.9}$$

Large values of R_s tend to reduce the gradient of the log-linear curve at the high forward-bias region and, hence, increase the n. Tunnelling through the device can also tend to increase the low forward bias current, decreasing the gradient of the log-linear I-V curve and, hence, increasing the n. When both effects are present in one device, the log-linear curve deviates accordingly, making the analysis more complicated. It should be noted that the largest gradient of this curve should be used to evaluate the smallest value of n and other parameters for accurate analysis of the device.

The intercept of the straight line with the highest gradient provides a more accurate value for I_0, and hence the ϕ_b present in the device can be evaluated from:

$$I_0 = SA^*T^2 \cdot \exp\left(\frac{-e\phi_b}{kT}\right) \tag{1.10}$$

This is a key parameter for a rectifying diode, and the production of an interface with a large ϕ_b is desirable for making an efficient PV cell. In addition, the depletion region and the interface should have minimum amounts of R&G centres to produce a high-quality PV cell, minimising the detrimental leakage process through the barrier.

By plotting I-V data measured under dark conditions, in a linear-linear graph (as in Fig. 1.11), series resistance (R_s) and shunt resistance (R_{sh}) can also be estimated from the forward and reverse current portions respectively. Therefore, the dark I-V measurements provide the most important parameters (n, ϕ_b, R_s, and R_{sh}) for the device structure and provide the quality of the depletion region and the information on current transport mechanisms in the device via the parameter n.

These parameters then help in establishing an equivalent circuit for the solar cell device, as shown in Fig. 1.12.

1.5.2 *I-V Characteristics of a Solar Cell Under Illuminated Conditions*

The directions of electron flow under dark and illuminated conditions are shown in the band diagrams in Fig. 1.13. This shows

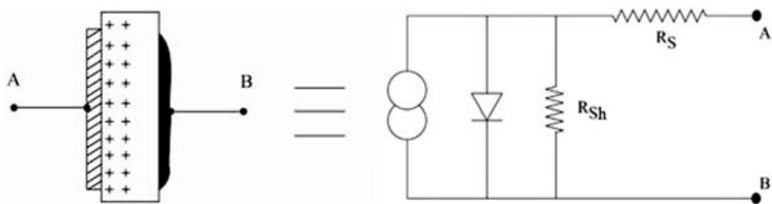

Figure 1.12 A schematic diagram of a Schottky barrier solar cell and its equivalent circuit.

that the photo-generated current flows in the opposite direction to the forward current under dark conditions. Therefore, the current through the diode under illumination is given by

$$I_\text{L} = I_\text{D} - I_\text{sc} = I_0 \cdot \exp\left(\frac{eV}{nkT}\right) - I_\text{sc} \tag{1.11}$$

where I_sc denotes the short circuit current produced by the solar cell under illumination.

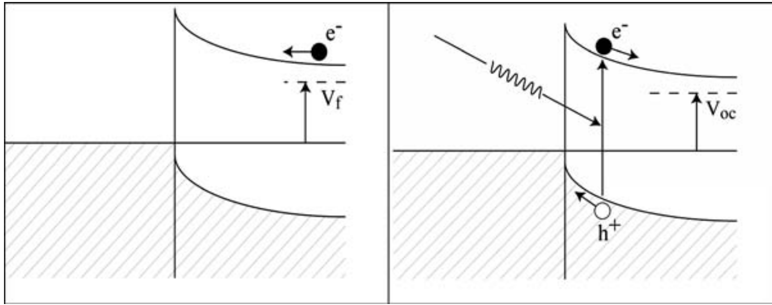

Figure 1.13 The direction of electron flow during forward bias under dark conditions and when used as a solar cell device under illuminated conditions.

The I-V characteristics described by Eqs. 1.6 and 1.11 can then be plotted in a linear-linear graph, as shown in Fig. 1.14. There are four important parameters to consider for a solar cell device.

- Open circuit voltage (V_oc): This is the voltage measured when the external circuit is in open condition, or when there is no current flow in the external circuit.

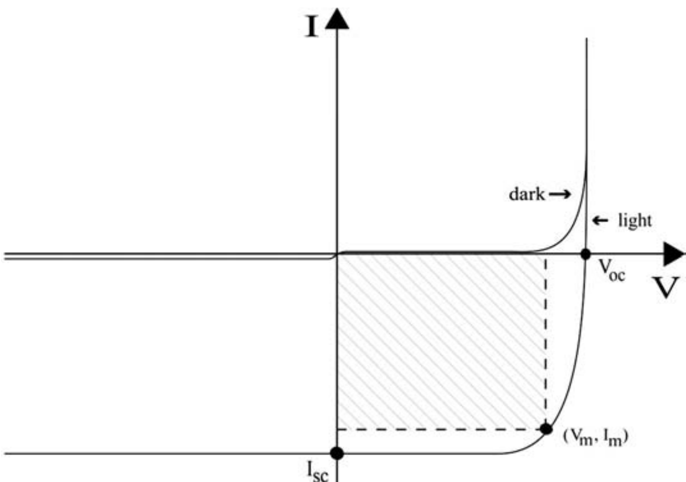

Figure 1.14 I-V characteristics of a PV solar cell under dark and illuminated conditions.

- Short circuit current density (J_{sc}): This is the current density produced when the two contacts are short circuited, or when there is zero voltage across the two contacts. This parameter is expressed as $mAcm^{-2}$ for convenience and provides easy comparison between devices fabricated with varying contact areas.

$$\left(J_{sc} = \frac{I_{sc}}{S}\right) \quad (1.12)$$

- Fill factor, or the curve factor (FF): This is a fraction defined to indicate the shape of the curve or the fraction of electric power that can be extracted from the solar cell. Therefore, the FF is defined as

$$\mathrm{FF} = \frac{V_m I_m}{V_{oc} I_{sc}} \quad (1.13)$$

  where V_m and I_m represent the parameters at the maximum power extraction point (V_m,I_m).
- Conversion efficiency (η): After defining the above three parameters, the light to electric power conversion efficiency is defined as

$$\eta = \frac{\text{Output Power}}{\text{Input Power}} = \frac{V_m I_m}{P_{in}} = \frac{V_{oc} \cdot I_{sc} \cdot \mathrm{FF}}{P_{in}} \quad (1.14)$$

when P_{in} is taken as the solar power incident on a unit area. The I_{sc} should be replaced by the current density (J_{sc}), giving

$$\eta = \frac{V_{\text{oc}} \cdot J_{\text{sc}} \cdot \text{FF}}{P_{\text{in}}} \tag{1.15}$$

The standard AM1.5 condition provides the value of $P_{\text{in}} = 100$ mWcm^{-2} as the solar constant to evaluate the efficiency of the device.

1.5.3 *How to Maximise V$_{oc}$*

The open circuit voltage achievable from a given junction depends on the electronic properties of that interface. In order to obtain an expression for the V_{oc} of a Schottky barrier solar cell, the diode characteristics under illumination (Eq. 1.11) can be used:

$$I_{\text{L}} = I_0 \cdot \exp\left(\frac{eV}{nkT}\right) - I_{\text{sc}} \tag{1.11}$$

By definition, $V = V_{\text{oc}}$ when $I_{\text{L}} = 0$, or the external circuit is kept open, or the current through the external circuit is zero. This gives

$$0 = I_0 \cdot \exp\left(\frac{eV_{\text{oc}}}{nkT}\right) - I_{\text{sc}}$$

or

$$SA^*T^2 \cdot \exp\left(\frac{-e\phi_{\text{b}}}{kT}\right) \cdot \exp\left(\frac{eV_{\text{oc}}}{nkT}\right) = I_{\text{sc}}$$

The rearrangement of this equation provides

$$V_{\text{oc}} = n\left[\phi_{\text{b}} + \frac{kT}{e} \cdot \ln\left(\frac{J_{\text{sc}}}{A^*T^2}\right)\right] \tag{1.16}$$

This indicates that the magnitude of V_{oc} depends on the value of the ϕ_{b}, present at the interface. Therefore, to achieve high values of V_{oc}, large potential barriers are desirable.

It is also evident that the V_{oc} depends on the value of n, the ideality factor of the diode. The value of n for an ideal Schottky diode with current-transport dominated by thermionic emission [13] is equal to unity ($n = 1.00$). But with current-transport dominated by R&G, n value is equal to 2.00, indicating a helpful parameter to

improve V_{oc}. But in real devices, J_{sc} is drastically reduced and, hence, V_{oc} decreases.

There is another factor which affects the value of n of a Schottky diode. In the case of metal-insulator–semiconductor (MIS)-type interfaces, the n value and ϕ_b increase as the insulating layer is incorporated and this effect helps in increasing the V_{oc} of a solar cell device [15].

In addition, the temperature of the cell also affects the V_{oc}. As the temperature decreases, the V_{oc} value increases due to minimisation of the thermal agitation of charge carriers. Therefore, in order to increase the V_{oc} of a Schottky barrier–based solar cell, improvement of the ϕ_b by the incorporation of an insulator, the reduction of the temperature of the cell, and the minimisation of the R&G process within the cell structure are desirable.

1.5.4 *How to Maximise J_{sc}*

The short circuit current density depends on the number of photo-generated charge carriers and their separation and collection rates in the external circuit. This requires efficient photon absorption from almost all regions of the solar spectrum by the materials used, effective carrier generations, and the high quality of the depletion region formed and hence the strength of the built-in electric field created. To increase the photo-generated charge carriers, impurity PV effect and impact ionisation can be combined together. With the right device design, the impurity PV effect can be used to create e-h pairs using surrounding heat energy. These will be described later, in chapters 6, 7, and 8, and are demonstrated by the latest experimental results. In addition, the detrimental R&G process and any other leakage paths must be removed from the device structure. To maximise the value of J_{sc}, the series resistance of the complete device must be minimised.

1.5.5 *How to Maximise FF*

To improve the shape of the I-V curve, and hence the FF, the total series resistance should be minimised (ideally $R_s = 0$). This includes resistance introduced by the electrical contacts, interfaces within

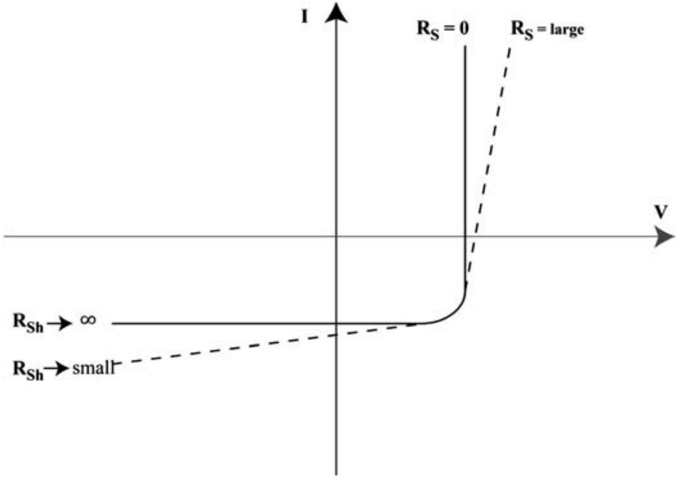

Figure 1.15 The effect of R_s and R_{sh} on I-V curves of PV solar cells.

the device, and materials used. The leakage resistance (or the shunt resistance) must be increased (ideally $R_{sh} \rightarrow \infty$). This can be achieved by minimising the R&G process and plugging any pinholes and other conducting paths in the material (Fig. 1.15).

1.6 Next-Generation Solar Cells

Next-generation solar cells will be developed based on various systems. Some of these devices are based on organic materials, dye-sensitised systems, and nanomaterials. However, the next stages of solar cells based on the most matured materials — inorganic semiconductors — have the highest potential to contribute towards solar energy conversion. This book, therefore, concentrates only on next-generation solar cells based on inorganic materials.

The basic interfaces used in solar cell devices are briefly described in this chapter. The next stage is to move forward and combine these basic interfaces to form more advanced PV devices. The aim is to effectively absorb the photons in almost all parts of the solar spectrum, create as many e-h pairs as possible, utilise other possible mechanisms such as impact ionisation and impurity

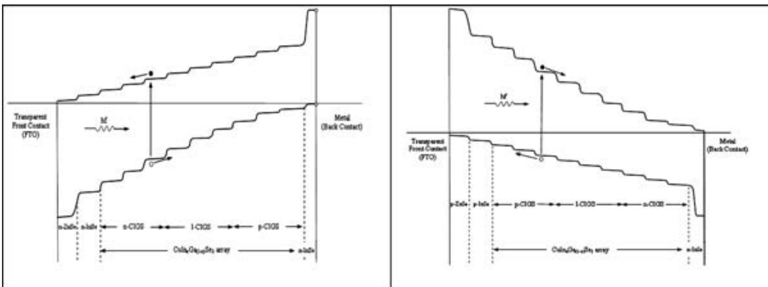

Figure 1.16 Multi-layer graded bandgap solar cell structures possible on n-type and p-type window materials.

PV effect to increase charge carriers, minimise R&G mechanisms, and effectively separate and transport charge carriers through the external circuit. The best candidate to satisfy all these conditions is the graded bandgap multi-layer solar cell structure, as shown in Fig. 1.16, based on n-type and p-type window materials. Chapters 6, 7, and 8 are devoted to the discussion of these devices together with the latest experimental results to indicate their high potential.

It may be useful at this stage to note that the graded bandgap structures are based on a large number of p-p- or n-n-type hetero-junctions and two ohmic contacts to the front and the back of the device. The front of the solar cell has wide bandgap n-type or p-type material, and the bandgap gradually decreases as it progresses towards the back of the solar cell. The electrical conduction type also gradually changes from n-type to p-type or p-type to n-type through the body of the device structure. The devices based on p-type window materials have potential barriers for electron transport, approximately equal to the bandgap of the wide bandgap window material, and hence the highest achievable ϕ_b. This means that the structures on p-type window materials are capable of achieving the highest possible V_{oc} value since it is a function of the ϕ_b.

1.7 Summary

PV solar energy conversion consists of four main stages — (a) absorption of a major part of the solar spectrum, (b) effective

creation of charge carriers (e-h pairs) within the PV device, and (c) separation of (e-h) pairs before their recombination — in order to (d) pass through an external circuit to create useful power. To achieve these four functions simultaneously, an electronic device containing a suitable interface with a built-in electric field is necessary. Such an interface can be an MS Schottky contact, a p-n homo-junction, a p-n hetero-junction, an n-n hetero-junction, or a p-p hetero-junction. MS and p-n junctions can be further modified to form MIS and p-i-n junctions respectively to enhance their performance. To produce an efficient PV solar cell, two or more interfaces mentioned above can be combined to form one solar cell structure. The graded bandgap multi-layer solar cell structures are the way forward to improving solar energy conversion in the future.

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Chapter 2

Status Report on Solar Energy Technologies

2.1 Introduction

The energy radiated from the sun is equivalent to a million billion 100 GW power stations. Part of this energy reaches the planet Earth at a rate of $\sim$1 kWm^{-2}, but technology has succeeded in tapping only a tiny fraction of this energy to date. The sunlight falling on Earth consists of ultraviolet (UV), visible, and infrared (IR) (heat) radiation, and all renewable energy sources (hydro, wind, waves, biomass, etc.) arise due to the primary solar energy.

The PV effect was discovered by a French scientist, Edmund Becquerel, in 1839, when he was 19 years old. Edmund may have learned this subject area from watching his father, Cesar, known as the grandfather of electrochemistry, working with electrodes and electrolytes in his laboratory (Fig. 2.1).

Although the PV effect was discovered in 1839, considerable effort was not devoted to developing this until the 1950s. As an energy conversion method, the use of PV technology was not considered during the industrial revolution, with cheap coal and oil being available, and the future damage to the environment was not

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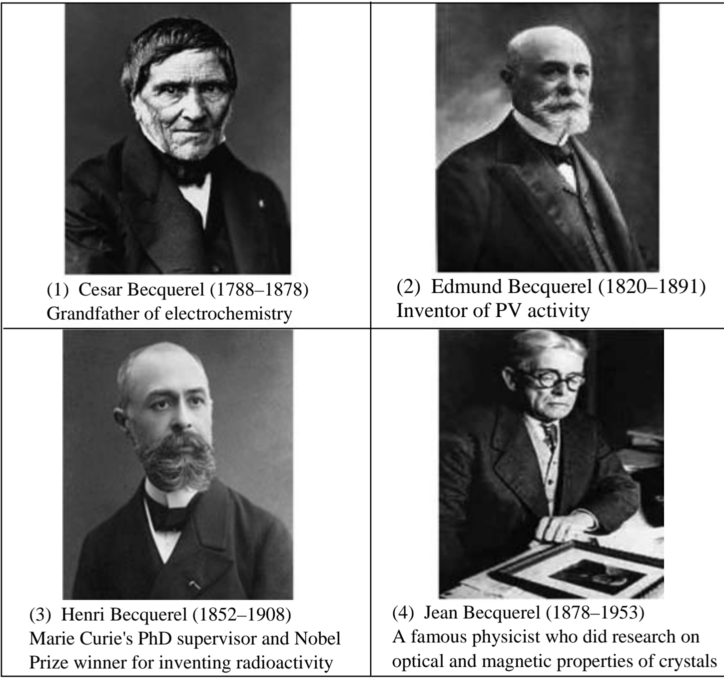

Figure 2.1 The inventor of the PV effect, Edmond Becquerel was the second in four generations of a family of famous French physicists.

Table 2.1 A time line of PV solar energy technology

1839:	The PV effect was discovered by Edmund Becquerel when he was 19 years old.
1883:	The first solar cell using elemental Se as the light-absorbing material was developed.
1916:	Millikan provided experimental proof of the photoelectric effect.
1918:	Czochralski developed a method to grow single-crystal Si.
1923:	Albert Einstein won the Nobel Prize for explaining the photoelectric effect.
1954:	4.5% efficient Si solar cells were produced at Bell labs.
1959:	10% efficient Si cells were produced, and the satellite *Explorer-6* was launched by the United States with a PV array of 9,600 cells.
1960:	14% efficient Si solar cells were produced by Hoffman Electronics.
1970s:	The first oil crisis kick-started the search for low-cost alternative systems for terrestrial energy conversion, accelerating PV research activities.
1980s:	Thin-film CdTe and CIGS solar cells were introduced into the mainstream of PV research.
1990s:	Dye-sensitised solar cell (DSSC) was introduced.
2000s:	Organic solar cells were introduced to the PV field.

envisaged at the time. But the relevant scientific research continued, and the main breakthroughs made are shown in Table 2.1 [1]. The first PV solar cell, with an efficiency of 4.5%, was produced in 1954 at Bell laboratories in the United States [2]. By 1960, 14% efficient Si solar cells were commercially produced and used in space applications. The first oil crisis, in 1970, kick-started the search for low-cost alternative methods for terrestrial energy conversion, and PV research was accelerated throughout the world.

2.2 Si Solar Cell Technology

The fabrication of the interfaces required for PV devices, as described in chapter 1, needs a light-absorbing electronic material with the desired semiconducting properties. The most widely used material is Si, and it has undergone over 60 years of research and development. The main steps of growth of Si and device fabrication are given in Fig. 2.2. Si is produced starting with natural sand (SiO_2), followed by four processing steps: (a) purification process, (b) crystallisation and wafer production, (c) processing of Si solar cells, and (d) assembly of the solar panels. This needs four different production lines, and these are summarised in Fig. 2.3 and Table 2.2. Each of these average-sized (∼25 MW) production lines could cost millions of dollars for the initial establishment. In addition, the whole process of converting sand into solar panels requires the heating of Si above its melting point (1,414°C), and repeated heating to high temperatures above 1,000°C, during solar cell fabrication. These steps demand a high energy input, burning fossil fuel, and therefore cost reduction is a challenging task for the Si PV industry.

Figure 2.4 shows the main stages of the manufacturing process of solar panels based on crystalline Si: the growth of a monocrystalline cylindrical crystal boule using Czochralski method, grinding of the crystal boule in order to produce single-diameter Si wafers, and a fully assembled solar panel with crystalline Si wafers.

Figure 2.5 shows the main stages of the production process of multicrystalline Si solar panels and the appearance of thin-film solar panels manufactured with amorphous Si. By the appearance of the

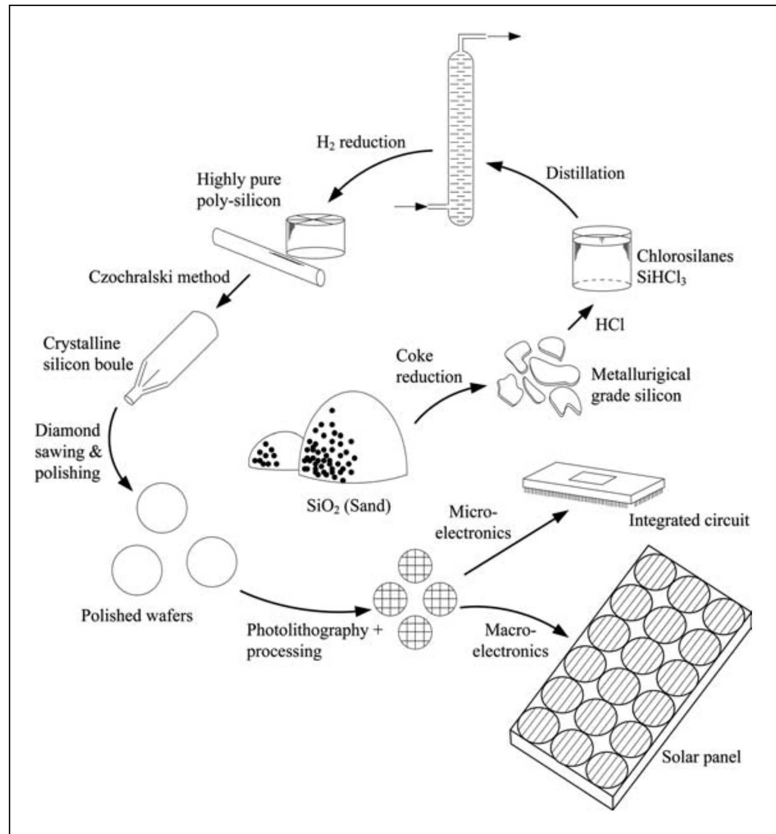

Figure 2.2 The main steps involved in the production of electronic-grade Si and device fabrication.

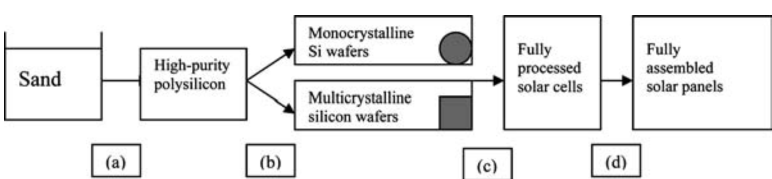

Figure 2.3 The four industrial production lines required for the manufacturing of solar panels based on crystalline and polycrystalline Si.

Table 2.2 Four industrial production lines involved in PV-technology based on Si

Production Line	Input	Output
(a) Si-purification line	Sand	High-purity polysilicon
(b) Si-wafer line	High-purity polysilicon	Mono- or multicrystalline Si wafers
(c) Si-cell line	Mono- or multicrystalline Si wafers	Fully processed solar cells
(d) Si-module line	Fully processed solar cells	Fully assembled solar panels

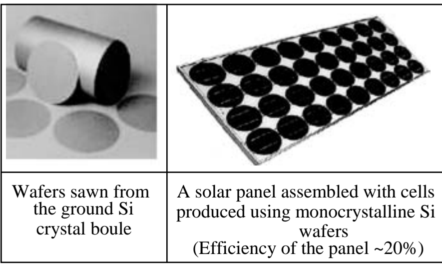

Figure 2.4 The main stages of the production of solar panels based on monocrystalline Si.

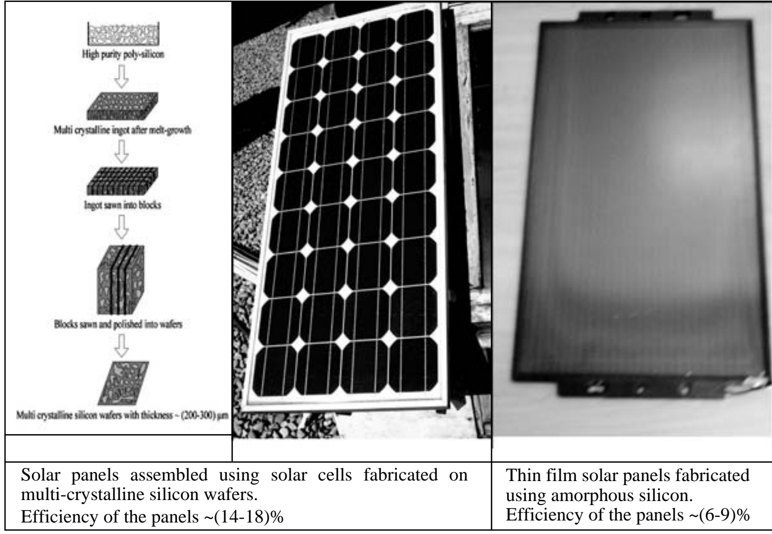

Figure 2.5 The appearance of solar panels based on polycrystalline Si wafers and amorphous-Si thin-film materials. See also Colour Insert.

final product, it is easy to recognise the three different types of solar panels produced using crystalline Si, polycrystalline Si, and amorphous Si.

2.3 PV-Manufacturing Cost Based on Si Technology

The cost of PV technology is given in \$/W, as shown in the following relationship:

$$\text{Cost of solar power}\left(\frac{\$}{W}\right)=\frac{\text{Production Cost}\Downarrow}{\text{Cell Efficiency}\Uparrow}$$

Both the reduction of production cost and the improvement of cell efficiency are challenging for Si technology, even after 60 years of research and development efforts. Si, however, dominates the PV industry because of the matured knowledge and established technology developed in this 60-year period. About 85% of the solar panels sold worldwide today are made of Si. The domination of Si will continue for some time, until real breakthroughs take place within alternative technologies and low-cost solar panels are manufactured on a large scale. Even with the high cost of PV technology, the size of the PV market is currently in excess of \$40 billion per annum and the market growth rate is over 45%. Some reports quote figures as high as ~68% for the growth rate of PV technology for the year 2004 [3].

In the early 1970s, the cost of PV solar energy production was over US\$20/W. This has been reducing continuously to a present value of ~US\$2–3/W. The PV-manufacturing cost reduction between 1980 and 2010 is given in Fig. 2.6, showing an impressive progress in the PV field. This reduction has been carried out by using all three Si technologies summarised above.

As the crystallinity reduces, the efficiency of cells reduces and the stability and lifetime suffers. Also, since the Si material is expensive, work is continuing to reduce the thickness of Si wafers from ~0.3 mm (300 μm) to ~0.15 mm (150 μm), but this has other detrimental consequences, such as the breaking of wafers in the production process. These are the main issues with Si technology, and, therefore, cost reduction is now progressing extremely slowly. However, numerous approaches to reduce material usage and increase the

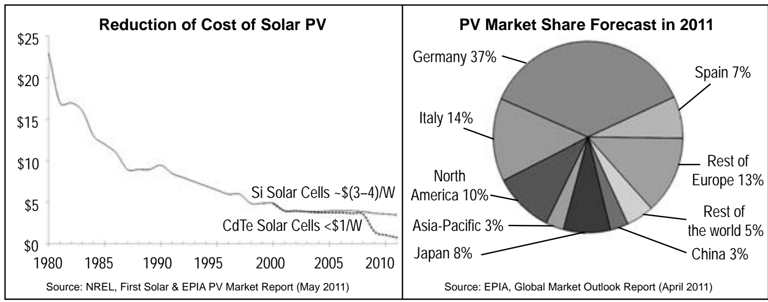

Figure 2.6 The reduction of cost of solar energy between 1980 and 2010 mainly using Si technology. See also Colour Insert.

efficiency of devices using this elemental semiconductor with many advantages are continuing in the research, development, and manufacturing stages.

PV solar applications are rapidly growing worldwide, but Japan, the US, and Germany are leading the way. China and India are introducing PV generation facilities rapidly, and Fig. 2.6 also shows the green world scenario in 2011.

2.4 PV Technology Based on III-V Compounds

In parallel to Si technology, high-efficiency solar cells have been produced using III-V semiconductors such as GaAs, AlGaAs, AlGaP, and InAs. These materials have been used to produce complex device structures with many material layers involved (see Fig. 2.7). Tandem solar cells using tunnel-junctions were proposed in 1979 [4] and practiced to date to develop these solar cells. The work in this field has produced impressive ~40% conversion efficiency to date, but there is huge potential to improve this further. A disadvantage of this device structure was pointed out by the author in 2005 [5–7], and the removal of this disadvantage will increase the efficiency well beyond 40%. This will be described in details in chapters 6, 7, and 8 of this book. The growth of III-V semiconductors needs techniques such as molecular beam epitaxy (MBE) and metalorganic chemical vapour deposition (MOCVD), which are prohibitively expensive in the production of PV modules technology for terrestrial

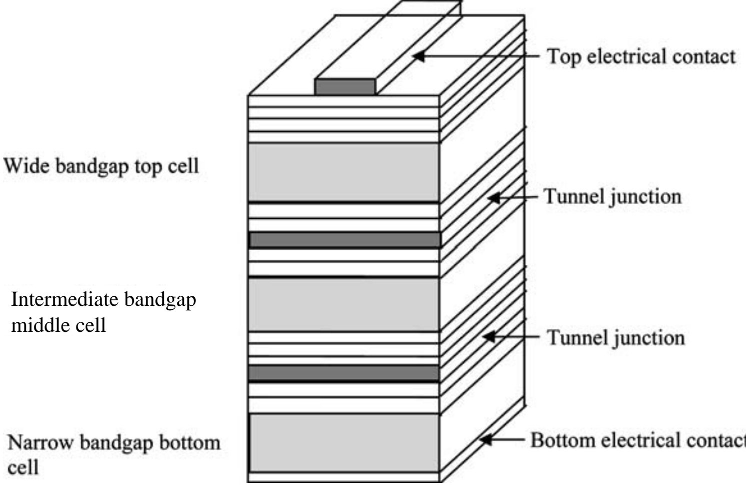

Figure 2.7 Complex and expensive solar cell structures based on III-V semiconductors, mainly developed for space applications and concentrator solar cells.

applications. However, these devices will have applications in the space industry and in solar panels with light concentrators. In addition, these well-researched III-V semiconducting materials help in the testing of new designs in PV devices.

2.5 New Technology for PV and Nano-Devices

Scientists have researched the electrodeposition of semiconductors over the past three decades and have grown many different semiconductors using this technique. The low cost, simplicity, scalability, and manufacturability of this method are attractive for large-area macroelectronic device ($\sim$1 m^2) manufacturing. The electroplating of II-VI semiconductors was first introduced by Kröger and Pannicker [8] in the late 1970s, and BP Solar started the scaling-up process in the mid 1980s and the manufacture of solar panels in late 1990s. Although the device understanding was based on a simple p-n junction during this period, solar panels of up to 0.94 m^2 with 10.4% efficiency were manufactured by

BP up to 2001. This is an outstanding achievement in thin-film solar panel manufacturing, but BP terminated this technology in 2001–2002 together with several other Si technologies as part of a rationalisation programme. This project successfully demonstrated the possibilities for full-scale manufacturing of $\sim$1 m^2 solar panels using electrodeposition.

The author was working in the research and development team of this solar panel at BP-Research Sunbury, London, in the late 1980s. Later, he continued his research at Sheffield Hallam University and, over the past 20 years, has explored the deep science behind the electrodeposited materials and PV devices. After comprehensive work carried out in many aspects of solar cells, six new patents have been secured based on new findings and results have been openly published [9, 10] for CBD grown CdS/electrodeposited CdTe solar cells. In this work, a new device concept was proposed, based on a combination of n-n hetero-junction and a large Schottky diode in the device instead of conventional p-n junction structure [10]. The details of this development and the new model proposed for high efficiency solar cells are presented in chapter 4.

First Solar announced in 2008 the achievement of US$1/W for thin-film solar panels based on vacuum-evaporated CdTe. This company is now leading with thin-film CdTe solar panels, exceeding 1 GW production in the year 2009. Electrodeposited CdTe solar panels show high potential for further reduction of the manufacturing cost, well below US$1/W.

2.6 Emerging Low-Cost Thin-Film Technologies

The alternative to expensive Si solar panels may come from thin-film solar cells based on CdTe, CIGS, DSSC, and organic solar cells. These four new technologies use simple techniques such as electrodeposition, chemical bath deposition (CBD), and screen printing for materials growth and temperatures below 500°C for device processing. These methods also minimise the use of expensive vacuum systems. The manufacturing of these solar panels needs only one production line in addition to required precursors,

Table 2.3 The lab-scale solar cell efficiencies and commercial-scale solar panel efficiencies for different PV technologies available to date. The figures given are approximate values for comparison

	PV Solar Technology	Research Period Devoted (in years)	Highest Efficiency Reported for Lab-Scale Devices (in %)	Efficiency Range for Large-Area Solar Panels (in %)
1	(a) Monocrystalline Si	~60	~25	18–23
	(b) Multicrystalline Si		~18	12–17
	(c) Amorphous Si		~14	5–10
2	III-V Compounds	~50	~40	—
3	CIGS thin-film solar cells	~30	~20	10–13
4	CdTe-based thin-film solar cells	~30	~17	10–14
5	DSSCs	~20	~12	5–6
6	Organic solar cells based on conducting polymers	~10	~8	—

instead of the four separate production lines required for Si technology. This has the potential to make a huge contribution to cost reduction in the future.

The lab-scale small-device solar cells and large-area commercial efficiency values are indicated in Table 2.3. Although CIGS-based solar cells achieved 20% efficiency at lab scale, the commercialisation rate is comparatively slow. The reason has been the difficulty in materials growth reproducibility due to the involvement of four elements in this alloy material. All other devices are also progressing forward, but CdTe commercialisation is very impressive. A US company, First Solar, has produced ~1 m^2 solar panel with ~10–14% efficiency and is rapidly ramping up its manufacturing capacity. After establishing the first production line in the US, First Solar now has plants in Germany and Malaysia and is spreading out to many other countries. The production volume is impressive, exceeding 1 GW per annum in 2009.

In the past, the use of Cd in PV solar cells was considered a hazard. However, this perception has now completely reversed. The world produces about 22,000 tonnes of Cd annually as a by-product of Zn and Cu processing [11]. A proportion of this is

used in Ni-Cd batteries, but the rest is not used and could end up polluting the environment. Locking up this toxic heavy metal in a less toxic CdTe compound, and making use of this compound to manufacture solar panels to produce clean energy, has been recognised as a good solution. Many research groups are now concentrating on the research, development, and commercialisation of CdTe PV technology using low-cost techniques such as close-space sublimation and electrodeposition. DSSCs are in the scaling-up stage, and organic solar cells are in their infancy. All technologies based on CdTe, CIGS, DSSC, and organic materials are moving forward with commercialisation programmes.

2.7 Summary

This chapter presented the current status of different solar energy technologies briefly and compared the approximate performance of each technology. Solar panels based on Si, III-V compounds, and thin-film solar cells based on CdTe, CIGS, dye-sensitised materials, and organic polymers are presented. Si solar panels dominate the market place at present, covering over 85% of the panels used. The recent developments in CdTe commercialisation by First Solar are gradually increasing the momentum of the take-up of thin-film solar cells. CIGS and DSSC solar panels will also enter the energy conversion market, while organic solar cells find their own niche applications in the field. By looking at the size of PV solar energy market, all solar technologies entering into the field will contribute to the clean energy production process in the future.

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Chapter 3

Electrochemical Deposition of Solar Energy Materials

3.1 Introduction

Semiconducting materials provide the main functions of a photovoltaic (PV) device, namely the optical absorption and creation of rectifying junctions to convert light into electricity. Therefore, the establishment of a suitable materials growth technique is essential in the PV development process. Various semiconductor growth techniques have been developed in the past for microelectronic devices ($\sim$1 μm^2). The melt growth or Bridgman technique, molecular beam epitaxy (MBE), metalorganic chemical vapour deposition (MOCVD), and their modifications are well known as high-quality semiconductor growth techniques. However, these techniques are not suitable for manufacturing macroelectronic devices ($\sim$1 m^2), such as PV panels and large-area display devices. Semiconductor growth techniques such as sputtering, close-space sublimation, electrochemical deposition, chemical bath deposition (CBD), spray pyrolysis, and their modifications have been developed to grow large-area thin films for these purposes. This chapter is devoted to providing a background to the electrochemical semiconductor

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growth technique, otherwise called the electrodeposition (ED) technique. For PV development, the technology used should be low-cost, scalable and manufacturable in order to produce low-cost solar panels for terrestrial energy conversion. The electrodeposition satisfies all three criteria mentioned above, and hence it is worth exploring and developing this technique for the production of solar energy materials and solar cells.

The electrodeposition of single elements, especially metals, is a well-established subject and has been used for centuries in the extraction of metals from their natural ores and in the coating of jewellery with noble metals, such as gold and silver. However, the use of electrodeposition for growth of semiconducting materials was first introduced after the late 1970s [1–5]. The work on the electrodeposition of II-VI semiconductors in the early 1980s led to the fabrication of CdS/CdTe solar cells based on electrodeposited CdTe layers [6]. In the early 1980s, the production of a thin-film solar cell with lab-scale device efficiency greater than 8% was a remarkable achievement and has during the past three decades stimulated worldwide research interest in the electrodeposition of semiconductors. The work has spread into many other materials, such as III-V, I-III-VI_2, organic polymers, and other alloy semiconductors. There have also been attempts to grow elemental semiconductors such as silicon [7] and mechanically harder materials like nitrides [8]. This chapter reviews the strengths, advantages and disadvantages of this simple but powerful technique in the development of macroelectronic devices such as PV solar panels and large-area display devices [9].

3.2 Electrodeposition of Semiconductors

The electrodeposition of semiconductors requires an electrolyte containing appropriate ions and three electrodes, as shown in Fig. 3.1 [10], or a simple two-electrode system eliminating the reference electrode. Consider $CuInGaSe_2$, a commonly used solar cell material, as an example. This material growth process needs an aqueous solution containing positive ions of copper, indium, gallium and selenium. Once a small DC power, typically in the mW range

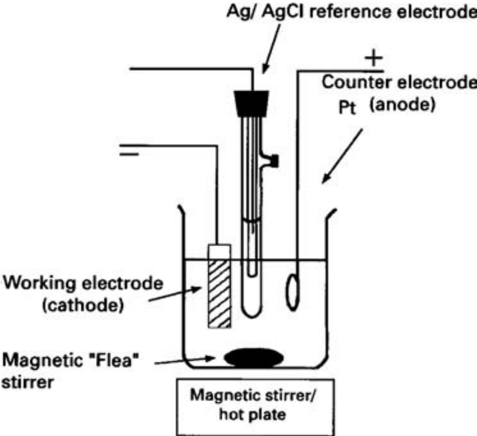

Figure 3.1 A schematic diagram showing the main features of a simple electrolytic cell used for the electrodeposition of semiconductors.

(∼2 V and ∼1 mA), is applied across the lab-scale-size anode and a cathode, the positive ions are attracted to the cathode, electrically discharged, and chemically reacted to form the material $CuInGaSe_2$. The working electrode (cathode) is usually an electrically conducting surface, and in the solar cell development, glass/conducting glass is a convenient substrate. The material properties depend on a number of parameters, such as ionic concentrations, electrodes used, the pH value, the stirring rate, the temperature, the nature of the substrate, the deposition voltage and the time. The optimisation of these parameters allows growers to produce semiconducting layers with the desired structural, mechanical, electronic and optical properties. Aqueous solutions enable growth temperatures varying from room temperature up to ∼85°C, and other non-aqueous media such as ethyleneglycol and dimethylsulfoxide (DMSO) allow an increase in temperature up to ∼170°C. The initial current-voltage (I-V) curve of the electrolyte, or the voltammogram, helps in estimating the approximate growth voltages of different phases of materials. With this information, growth voltages can be optimised to produce layers with desired properties. The material layers grown by electrodeposition are usually amorphous, nano- or microcrystalline, and therefore this method is a convenient technique for the growth

of materials for nanotechnology research and applications. In rare situations, crystalline materials (e.g., ZnSe) are also possible from this technique. The deposition of consecutive semiconducting layers enables in some cases the fabrication of complete electronic devices within one electrolyte, as explained later in this chapter.

3.3 Strengths and Advantages of Electrodeposition

3.3.1 *Simplicity, Low-Cost, Scalability, and Manufacturability*

Electrodeposition is usually carried out in normal laboratory conditions without the requirement of a vacuum system. Low-temperature growth saves energy, but most of the electrodeposited material layers need a post-deposition annealing step at an optimised elevated temperature of around 400°C in a suitable atmosphere for approximately 15 minutes. The low-temperature electrodeposition allows the fabrication of abrupt junctions, minimising interactions at these interfaces during growth.

The most attractive feature is the low cost when compared to other semiconductor growth techniques. A well-established MBE or MOCVD system needs an initial cost in the order of £1 million, and these systems have limitations as to the number of different materials which can be grown. These techniques have been developed in the past to grow small wafers of high-quality semiconductors to fabricate microelectronic devices. These techniques serve that purpose well although the costs are high. In the case of electrodeposition, a computerised potentiostat costs about £6,000 and a wide range of materials can be grown. The change of the electrolytic cell provides the conditions necessary for the growth of a new material.

For macroelectronic devices, such as solar panels and large-area display devices, scalability is very important. In the case of electrodeposition, it is possible to use large tanks as electrolytic baths and, therefore, large-area thin films can be produced. As shown in Fig. 3.2, batches of a number of large plates can

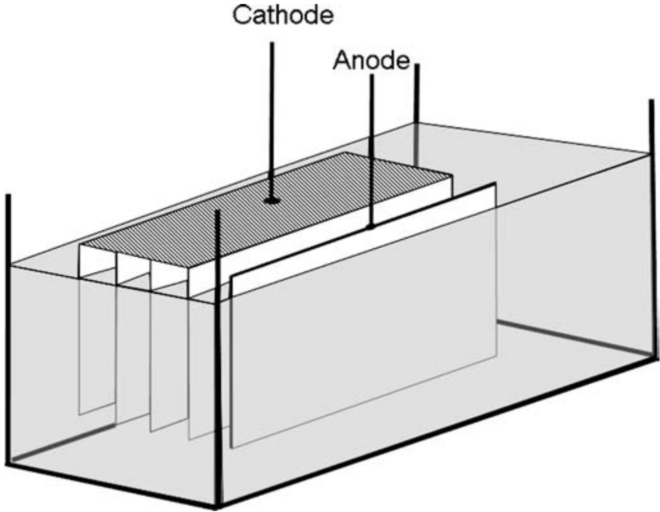

Figure 3.2 Electrodeposition is suitable for the processing of batches of large-area devices through multi-plate cathodic deposition. See also Colour Insert.

be prepared using this technique. The production of 0.9 m^2 solar panels by BP Solar using electrodeposited CdTe achieving efficiencies greater than 10% has proved the manufacturability of this technology. Recent accelerated work on electrodeposited solar energy materials and devices in many parts of the world [11–13] shows the recognition of the strengths of this simple technique.

3.3.2 *Self-Purification and Built-in Hydrogen Passivation*

In the development of electronic materials and devices, impurity control is a critical issue. The first step is to minimise the impurity sources present in and around the electrolyte. The solvent used in the electrolyte should be a high-purity medium, and in the case of aqueous solutions, double-distilled water or de-ionised water fulfils the requirement. In many situations, the electrolytes are acidic, with pH values in the range 2–4, and under these conditions, silicon and sodium ions leach into the electrolyte from glass vessels used for the electrolytic bath [14]. This can be easily eliminated by using Teflonware instead of glassware in the electrolytic bath.

The second step is to use the highest-purity chemicals available for the preparation of the ionic solutions. It is usual practice to use 5N or 6N (99.9999%) purity chemicals in all semiconductor growth techniques today. Electrodeposition, however, has an added advantage over other semiconductor growth techniques, which is the self-purification capability. Once the electrolyte solution has been prepared using the highest-purity chemicals available, the self-purification process can remove any background impurities from the electrolyte. An application of slightly lower voltage than the usual growth voltage over a suitable period prior to growth will enable subsequent growth of high-purity semiconducting materials. The purity of semiconducting layers improves as the material layers are plated from a given electrolyte due to the removal of impurities from the solution.

Hydrogen passivation and sulphur passivation are well-known phenomena in the growth of silicon and surface preparation of GaAs. The electrodeposition from aqueous solutions has a built-in hydrogen passivation mechanism since H^+ ions are also attracted to the surface of the cathode and discharged together with other semiconductor elements. Any dangling bonds formed during the formation of the semiconductor are immediately passivated by the most active hydrogen atoms produced after the discharge of H^+ ions. On various occasions, sulphur compounds are added to the electrolyte and, therefore, the passivation could also take place due to the incorporation of sulphur in these layers.

3.3.3 *Extrinsic and Intrinsic Doping*

Once the background impurity level has been reduced to a minimum, it is an easy task to apply extrinsic doping. A calculated amount of external dopant can be added to the electrolyte before the growth of any semiconducting layer. This has been applied to electrodeposition of ZnSe layers in recent research [15]. The conduction type of the thin films grown was determined using photoelectrochemical (PEC) cell measurements, as shown in section 3.4.3.

In the cases of II-VI and I-III-VI_2 materials ($CuInSe_2$, for example), intrinsic doping is possible by the variation of its composition. In the

stoichiometric $CuInSe_2$ material, 25% of the group-I element (Cu), 25% of the group-III element (In), and 50% of the group-VI element (Se) can be found. However, a slight increase of the group-I element makes the material p-type and a slight increase of the group-III element makes the material n-type in electrical conduction. The variation in electrical conduction through p^+, p, i, n, and n^+ has been established in 2006 for materials based on $CuInSe_2$ [16] and in 2007 for materials based on $CuInGaSe_2$ [17] and the results are summarised in section 3.4.3.

3.3.4 *Ability in Bandgap Engineering*

It is also possible to engineer the bandgap of alloy semiconductors, such as $CuInGaSe_2$. The bandgap of $CuInSe_2$ is $\sim$1.10 eV, and this value can be increased by adding gallium into the layers. Electrodeposition provides a convenient way of this required variation of gallium by changing the growth voltage. This property, therefore, can be used for the effective absorption of a major part of the solar spectrum using multi-layer graded bandgap structures (see Fig. 1.16 and chapter 6). These new device structures need gradual variation of the bandgap together with electrical conduction type change from p-type to n-type, or vice versa. The electrodeposition of $CuInGaSe_2$ simultaneously provides both these variations during the growth process [17].

3.3.5 *Other Advantages of Electrodeposition*

There are many other advantages in the electrodeposition of semiconductors. In techniques such as MBE and MOCVD, the phase changes occur directly from gas to solid during the materials growth process. However, in electrodeposition, phase changes occur from liquid to solid and nature prefers this transition and, therefore, should produce high-quality material layers. In addition, the available source of electrons at the cathode surface should provide better growth conditions, fulfilling the charge neutrality requirements during materials growth.

One other important feature of electrodeposition is the possibility of defect passivation in a wet chemical environment. As the

layers grow on the cathode surrounded by wet chemicals, unwanted defects can be removed from the material layer. The best example is the $CdCl_2$ treatment of CdS/CdTe solar cells in order to enhance efficiency values from ~3–5% to ~12% [18]. Although there is no agreed scientific understanding of this process to date, grain growth, doping, and defect passivation must be taking place during this wet treatment and annealing process. Electrodeposition provides an excellent tool for exploring new science and developing electronic materials, especially for fabricating large-area devices. This method can also be used to deposit materials on selected parts of electronic devices or circuitry with any shapes of the substrate.

3.4 Experimental Evidence

3.4.1 *Observations in XRD*

Electrodeposition of ZnSe and material characterisation results have been reported in detail [15]. ZnSe layers grown by electrodeposition and MBE have been studied by XRD under the same conditions for comparison. Figure 3.3 shows such an example, and close observation of the width of the most intense XRD peaks show that the crystalline property of the electrodeposited layers seems comparable, if not superior, to that of MBE-grown layers. It is also noteworthy that the electrodeposited layers are grown on polycrystalline indium tin oxide (ITO) substrates when compared to well-ordered GaAs (100) surfaces provided for MBE-grown ZnSe layers. Therefore, under optimised and favourable conditions, the electrodeposition technique is capable of producing high-quality electronic materials for some semiconductors.

3.4.2 *Observations in XRF*

An example of X-ray fluorescence (XRF) results for electrodeposited $CuInSe_2$ is shown in Fig. 3.4 [16]. This graph shows the variation of atomic percentage as a function of growth voltage for a two-electrode electrodeposition system. These results demonstrate that

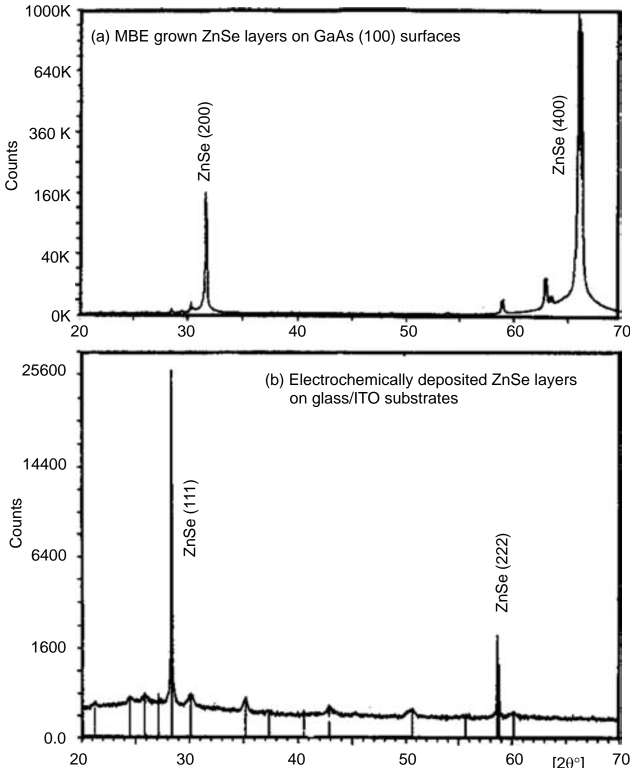

Figure 3.3 XRD patterns obtained for MBE-ZnSe layers grown on GaAs (100) surfaces and annealed films of electrodeposited ZnSe layers grown on glass/ITO substrates. Note that the electrodeposited ZnSe shows a high degree of crystallinity, and only the growth orientation is different for the two materials [15].

the composition of material layers can be produced simply by selecting the growth voltages. Also, the possibility of formation of different phases is evident from these experimental results. Proper optimisation and control of growth conditions could provide material layers with desired stoichiometry and properties. These results indicate that the electrodeposited $CuInSe_2$ layers are rich in copper at low growth voltages and rich in indium at high growth voltages, changing the composition of the material layers.

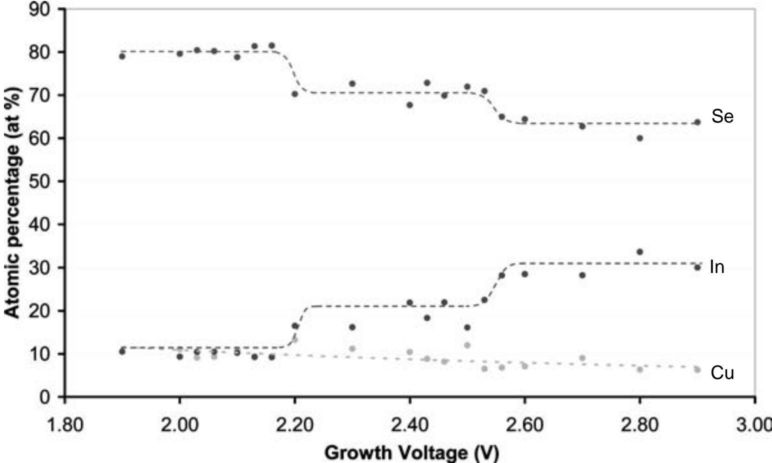

Figure 3.4 The atomic percentage of individual elements as determined from XRF for material layers grown at different voltages using a two-electrode system [16]. See also Colour Insert.

3.4.3 *Observations in PEC Cell Measurements*

Electrodeposited semiconducting layers are usually grown on conducting surfaces like glass/conducting glass substrates. The thickness of the electrodeposited layers can be in the sub-micron range (50–1,000 Å), and hence the determination of the electrical conduction type using standard techniques like the Hall effect is a challenging task. A solution to this is a simple PEC cell measurement.

A system like glass/conducting glass/semiconducting layer can be used to form a solid/liquid junction between the semiconductor and a suitable electrolyte. This junction is very similar to a Schottky diode formed at a semiconductor/metal interface. The only difference is the replacement of the metal contact with a conducting electrolyte. The open circuit voltage of this junction can be determined easily by measuring its voltage with respect to another electrode under dark and illuminated conditions. The difference between the two readings — the open circuit voltage of the solid/liquid junction — is the PEC signal, which can be used to identify the electrical conduction type of the semiconductor. The sign of the PEC signal determines the electrical conduction type, and

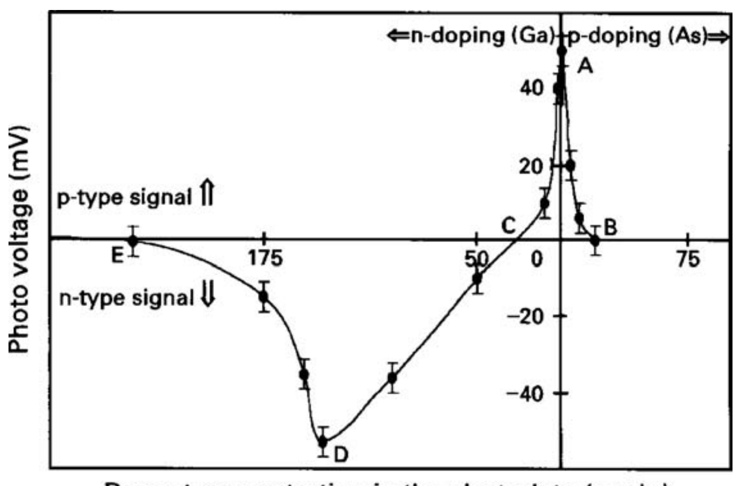

Figure 3.5 PEC results to show that ZnSe can be doped to produce both n- and p-type materials by adding relevant impurities into the electrolytic bath [15].

the magnitude indicates the quality of the depletion layer formed at the interface. Both metals and insulators show a zero PEC signal due to non-formation of a useful depletion region. Metals form extremely thin depletion layers, and insulators form extremely thick depletion layers, producing a zero PEC signal in both cases.

Figure 3.5 shows the ability of extrinsic doping of electrodeposited ZnSe layers [15]. An aqueous electrolyte containing 0.1M $ZnSO_4$ and 10^{-5}M SeO_2 forms p-ZnSe when grown at ~65°C with pH = 2.00~2.50. The figure shows the variation of a PEC signal as a function of external doping of the material. Undoped material indicates p-type conductivity, showing ~50 mV, as shown by the vertical axis of Fig. 3.5 (point A). The horizontal axis shows the amount of dopant added to the bath in parts per billion (ppb) level. However, it should be noted that the amount of dopant incorporated in the film can vary considerably, depending on the electrodeposition parameters. This will only guide the grower in producing the required doping levels. Addition of arsenic (As) into the solution gradually increases the p-type doping providing p^+ materials. As a result, the depletion region of the ZnSe/liquid

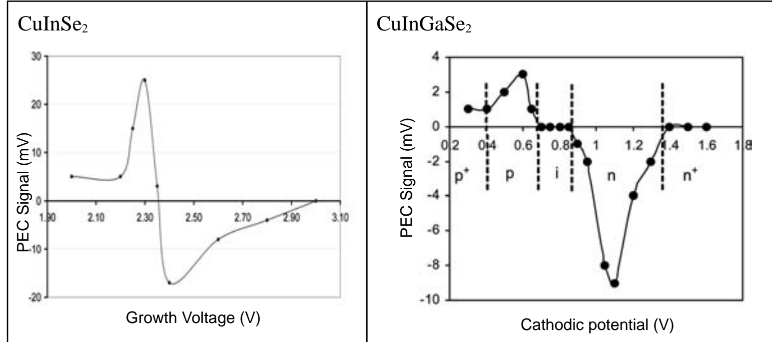

Figure 3.6 PEC signals observed for various samples of $CuInSe_2$ and $CuInGaSe_2$ materials grown at different deposition voltages. Note the ability to grow p^+, p, i, n, and n^+ materials from the same electrolyte, simply by varying the deposition voltage to alter material composition [16, 17].

junction diminishes and the positive PEC signal reduces to zero, as shown by the curve AB. On the other hand, doping with Ga by adding $Ga_2(SO_4)_3$ to the bath reduces the p-signal to zero (AC) due to compensation and increases the n-signal (CD) because of appropriate doping suitable for Schottky-type devices. Further addition of Ga heavily dopes the material, causing the depletion region to diminish and, hence, the n-signal to reduce to zero (DE). This clearly demonstrates that ZnSe can easily be doped to produce both n-type and p-type materials using the electrodeposition technique.

Figure 3.6 shows examples of intrinsic doping of semiconductors making use of their composition changes. Both $CuInSe_2$ [16] and $CuInGaSe_2$ [17] layers show p-type conduction when the material is rich in Cu at lower growth voltages. However, when the material is grown at higher cathodic voltages, layers become rich in indium, hence changing to an n-type material. The shape of the curve for $CuInGaSe_2$ is slightly different due to the presence of Ga in the bath. This property is extremely important since p-i-n structures can be fabricated using one electrolyte simply by changing the growth voltages of the material. For example, the p-i-n structure based on CIGS could be grown by applying voltages at 0.60 V, 0.75 V, and 1.10 V, in that order, for given time periods. Also, in the case

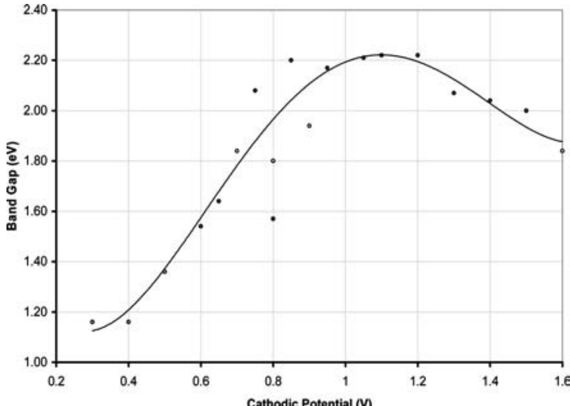

Figure 3.7 The variation of the energy bandgap between ~1.10 and 2.20 eV for electrodeposited $CuInGaSe_2$ layers grown as a function of cathodic potential [17].

of development of graded bandgap multi-layer devices, this is an excellent feature to exploit.

3.4.4 *Observations in Optical Absorption Measurements*

Optical absorption technique allows the determination of the energy bandgap of semiconductors. Figure 3.7 shows the measured bandgap values of $CuInGaSe_2$ layers electrodeposited as a function of cathodic potential, and it is clear that the bandgaps can be varied from 1.10 eV to ~2.20 eV by changing the deposition voltage [17]. The 1.10 eV bandgap is very close to $CuInSe_2$ grown at low cathodic voltages, and the bandgap increases as the cathodic potential increases, due to attraction of more Ga into the deposited layer. Again, this property can be used to develop graded bandgap solar cell structures.

3.4.5 *Observations in Photoluminescence*

ZnSe layers grown by electrodeposition and MBE techniques have been studied using photoluminescence under identical conditions in order to compare the defect levels present in their forbidden

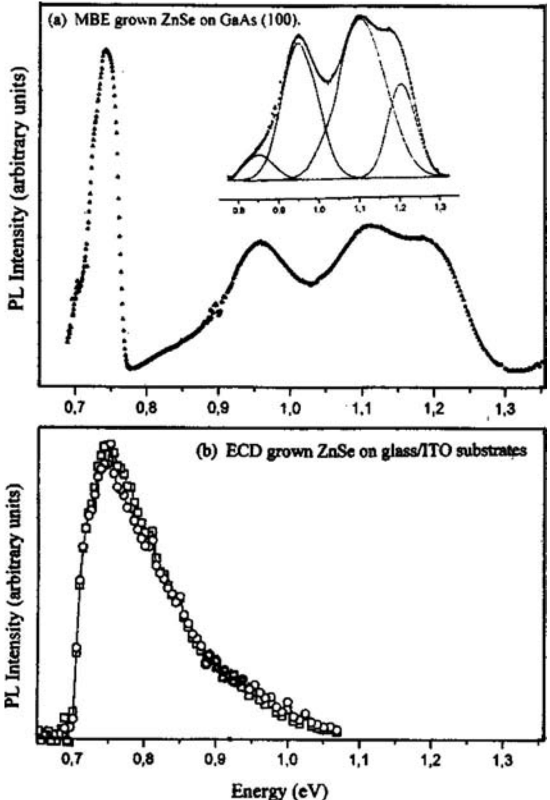

Figure 3.8 Photoluminescence spectra obtained for (a) ZnSe layers grown by MBE on GaAs (100) surfaces and (b) electrochemically deposited ZnSe layers on glass/ITO substrates [15].

bandgaps [15]. The results obtained are shown in Fig. 3.8 for comparison. It is evident that there are at least five defect levels in the observed energy range for MBE-grown ZnSe, but in comparison, there is only one defect level for electrodeposited ZnSe layers. The only difference is the broadened peak at 0.75 eV, possibly due to a distribution of energy levels at the vicinity of that defect level. However, the overall observation is that the electrodeposited layers possess much cleaner bandgaps than MBE-grown ZnSe layers used in these investigations. This example highlights the possibility of

production of electronic materials with enhanced defect passivation using wet chemical methods rather than dry vacuum techniques.

Similar observations have been made for electrodeposited CdTe layers using the deep-level transient spectroscopy (DLTS) technique [19]. When electrodeposition conditions are optimised, the number of DLTS peaks observed is minimum when compared to CdTe materials grown by other techniques.

3.4.6 *Impurity Control in Semiconductors*

A comprehensive study carried out on impurities in CdTe by Lyons *et al.* [20] also provides experimental evidence for high purity of electrodeposited CdTe layers. This group obtained CdTe from all possible growth techniques and carried out secondary ion mass spectroscopy (SIMS) profiling studies under similar conditions to investigate the impurities present in these materials. This work concluded by stating, 'Electrodeposition of CdTe has shown polycrystalline layers which were purer than the ultra-pure crystals bought as 4N, 5N or 5N+ materials from various commercial suppliers.'

This fact is also confirmed by fully processed CdS/CdTe solar cell devices produced with electrodeposited CdTe material. For solar cell devices showing efficiencies above 12%, the reverse breakdown voltage goes up to ∼32 V [21]. It is remarkable to observe these results for a ∼2 μm thick device structure, and these properties highlight the purity of CdTe material in these devices showing a large resistance to the reverse-bias breakdown process. An impure material will produce diodes with breakdown voltages at few volts in the reverse-bias region.

This experimental evidence demonstrates that electrodeposition with self-purification capability is producing high electronic quality CdTe materials. With optimised growth conditions, this method is capable of growing many other semiconducting materials.

3.5 Issues in Electrodeposition of Semiconductors

Electrodeposition from aqueous solutions limits the growth temperatures to a narrow range of 20–85°C due to the 100°C boiling point

of water. The use of non-aqueous solvents, such as ethyleneglycol and dimethylsulfoxide (DMSO), expands this temperature range to 20–170°C. Because of the low growth temperature involved, the thin-film materials obtained are usually amorphous, nano- or microcrystalline in nature. Crystalline materials are also possible only in special cases like ZnSe [15]. For electronic device applications such as photovoltaics, the electrodeposited layers must undergo a post-deposited annealing step in order to improve the crystallinity, electronic and optical properties. This can be seen as a disadvantage, but in semiconductor processing terms, heat treatment at ~400°C is still a comparatively low-temperature process.

Impurities in semiconductors play an important role in the development of electronic materials and devices. Therefore, the impurity levels should be controlled at parts per million (ppm) levels in many cases and parts per billion (ppb) levels in some cases. The impurity sources of electrodeposition technique include vessels, solvents, electrodes, and the chemicals used in the electrolytic cell. As discussed in earlier sections, leaching of sodium and silicon from glass ware in acidic media is a disadvantage but can be easily avoided by using Teflonware to contain the electrolyte. In the case of aqueous solutions, water can be purified adequately through deionisation and distillation processes. Non-aqueous solvents can be purified using electrodeposition itself prior to the preparation of solutions. Electrodes used need to be made out of inert elements such as platinum or high-purity graphite. The use of reference electrodes such as standard calomel or Ag/AgCl, may be problematic since these are sources of ions such as Hg^+ and Ag^+. These ions can be beneficial for certain materials but could poison the bath for some material systems. For example, Hg^+ ions are beneficial in improving cell performance [21] but Ag^+ ions have completely detrimental effects by reducing cell efficiencies for solar cells based on electrodeposited CdTe [22]. For this reason, electrodeposition has been tested successfully using the two-electrode system by avoiding the reference electrode [16, 17].

Another concern in electrodeposition is that the material layers grow on the cathode in the presence of other ionic species, such as OH^-, SO_4^{--}, Cl^- or NO_3^-. These ions could also be incorporated in thin films depending on the thermodynamic and kinetic conditions,

creating beneficial or detrimental effects. The incorporation of hydroxides in semiconductors can be a major issue when aqueous solutions are used. Due to the above reasons, one may not be able to grow some materials using aqueous media, but a large number of semiconductors [10] have been successfully grown to date using this method. Hydroxide incorporation can be avoided by using non-aqueous solvents like DMSO. However, over the past three decades, the lack of close collaboration between the two disciplines chemistry and physics has been a major barrier for rapid progress in electronic device development based on the electrodeposition of semiconductors.

One other disadvantage of electrodeposition is that the substrates are limited only to conducting surfaces. Materials cannot be deposited on insulating surfaces without having electrical conduction. Another complication is that the conducting layer on the substrate may dissolve in the acidic or alkaline electrolyte solutions used during the electrodeposition of the material.

3.6 Current Work and Future Prospects

The use of electrodeposition as a growth technique for solar energy materials and nanomaterials is getting more popular in the research community. The experimental results currently reported are impressive, and this simple technique allows the simultaneous variation of the bandgap of $CuInGaSe_2$ between 1.10 eV and 2.20 eV and the electrical conduction type from p^+ to n^+ by changing the deposition voltage. In addition, this method is capable of fabricating any number of electronic material layers necessary for solar cell devices. If these capabilities are used in the manufacture of large-area solar panels, the production cost could be reduced by a considerable factor in the future.

Making use of electrodeposited CdTe layers, small-scale device efficiencies of 18% for CdS/CdTe solar cells have been reported [23]. However, the reproducibility of these high-efficiency devices remains a real challenge for PV researchers. A deeper understanding of the electrodeposition process, material properties, device structures, and the underlying physics principles will help in

the establishment of reproducibility and consistency, increasing the device parameters further. The new science emanating from electrodeposition research, materials, and device understanding could also help the development of various electronic devices using other growth techniques [24].

Electrodeposited materials can be used to fabricate multi-layer graded bandgap solar cell structures due to the capability of changing conduction type and ability to engineer the energy bandgap simultaneously. The use of the latest knowledge in the electrodeposition of $CuInGaSe_2$ enables low-cost fabrication of these next-generation solar cells, as shown in Fig. 3.9. This is an n-i-p device structure grown using $CuInGaSe_2$ layers on glass/FTO/n-CdS surfaces. The n-i-p structure was grown using one electrolyte by applying voltages at 1.10 V, 0.75 V, and 0.60 V in that order (see Fig. 3.6) for predetermined time periods. In order to deposit equal thicknesses for three layers, the charge flow ($Q = It$) through the electrolyte can be set to a constant. This process simultaneously provides both electrical conduction type and the bandgap variation required for these multi-layer solar cell structures. By a simple computer programme, the number of layers can be increased to a large number to smooth out the edge of the energy bands.

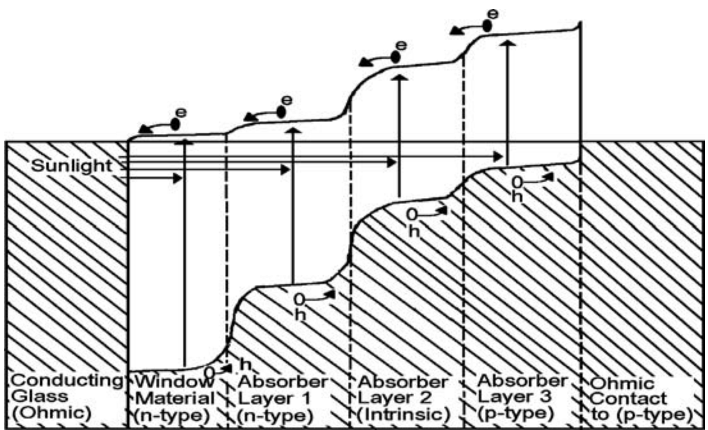

Figure 3.9 An energy band diagram of an n-i-p structure grown using $CuInGaSe_2$ on a glass/FTO/n-CdS surface to form an n-n-i-p device structure.

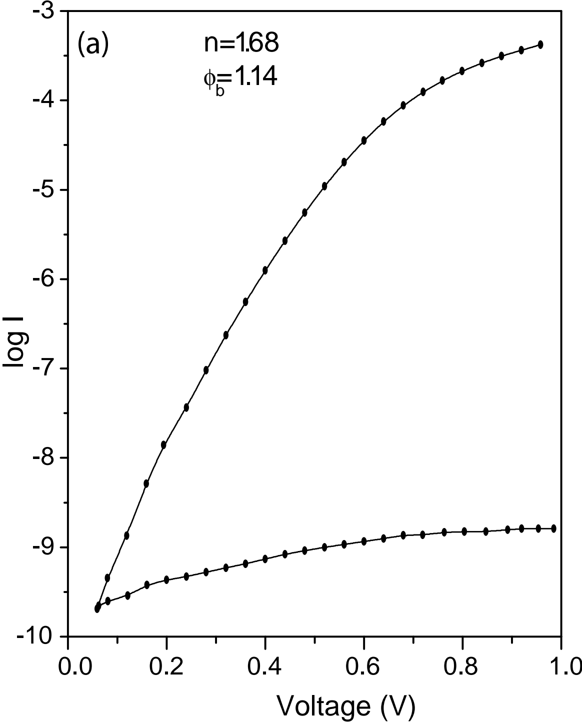

Figure 3.10 Typical log-linear I-V characteristics under dark conditions for an n-n-i-p structure shown in Fig. 3.9 and fabricated with electrodeposited layers. Note the RF of $\sim 10^6$, the n of 1.68, and the potential barrier height (ϕ_b) of 1.14 eV [17].

Figure 3.10 shows a dark I-V curve of a four-layer device fabricated using electrodeposition with an n-n-i-p structure, as shown by the energy band diagram in Fig. 3.9. This is an excellent diode with the rectification factor (RF) at 1.00 V, about six orders of magnitude, ideality factor (n) of 1.68, and a potential barrier of 1.14 eV. The future work should be directed towards research and development of these promising multi-layer graded bandgap solar cell structures using low-cost electrodeposited materials. The challenges faced by researchers are the consistency and reproducibility of materials growth due to the existence of four or five different elements in this alloy compound semiconductor.

Lab-scale devices show high promise, but the scaling-up remains a challenge for the PV research community to overcome uniformity, reproducibility, and yield issues.

3.7 Summary

This chapter reviewed the strengths, advantages, disadvantages, and future prospects of electrodeposition as a low-cost and large-area semiconductor growth technique for applications in macroelectronic devices such as solar panels and large-area display devices. To highlight its strengths, experimental evidence obtained from XRD, XRF, PEC, optical absorption, and photoluminescence have been presented. It has been shown that when materials are grown in optimised conditions, electrodeposition is capable of producing high-quality materials for electronic device applications. This chapter also demonstrated the possibility of the fabrication of graded bandgap multi-layer solar cell device structures using electrodeposited CIGS with promising device properties.

Electrodeposition satisfies all three criteria necessary for the research and development of PV solar cells. This technique fulfils (i) low-cost, (ii) scalability, and (iii) manufacturability and, therefore, is capable of cutting down the costs of solar panels drastically in the future. Many research groups are now reporting the highest-purity electrodeposited materials and the excellent qualities of thin-film devices made out of these materials.

These promising experimental results invoke systematic and focussed research efforts related to electrodeposited semiconductors, and this method has much to offer to the field of macroelectronics such as photovoltaics and large-area display devices and, in particular, to the new emerging area of nanotechnology.

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Chapter 4

Background of the CdTe Solar Cell and the New Device Concept

4.1 Introduction

Development of a low-cost thin-film solar cell device with a reasonable efficiency for terrestrial solar energy conversion has been the subject of active research over the past three decades. Two systems based on $CuInGaSe_2$(CIGS) and CdTe absorber materials are currently under intense research and development worldwide. CIGS-based solar cells are currently leading with record efficiencies of 20.3% [1], whereas CdTe-based solar cells have achieved 16.5% [2] for small-scale laboratory devices. The slow progress on the CdTe solar cell research front is noteworthy as it has taken eight years of worldwide research to increase the efficiency by only 0.6%, from 15.9% by Britt *et al.* in 1993 [3] to 16.5% [2] by Wu *et al.* in 2001. This efficiency figure has been stagnated around 16% since 1993.

Although the scientific understanding of material issues and device physics was slow and lab-scale device efficiency did not improve, impressive progress took place in parallel on the scaling-up and technology front. In commercialisation on the CdTe front, progress was faster than CIGS solar cells, and Antek, First Solar

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and BP Solar have been successful in manufacturing $\sim$1 m^2 solar panels based on CdTe. Both Antek and First Solar grow CdTe using close-space sublimation, but BP Solar grew CdTe using electrodeposition. Ramping up of manufacturing capabilities to over 1 GW per annum in 2009, First Solar made a huge stride in the thin-film solar panel production. Although BP Solar terminated CdTe solar panel manufacturing programme together with a few other solar technologies in 2001–2002, this production line successfully demonstrated the manufacturability of CdTe solar panels using electrodeposition [4].

Since manufacturing capabilities are well established in the industry, what is now required is to improve the understanding of material issues and physics behind these devices in order to increase the conversion efficiency. This process will rapidly reduce the $/W figure well below $1/W. This chapter briefly presents the conventional device model used to describe the PV activity of CdTe solar cells and introduces an alternative concept to describe the device structure using advances that took place in the research field. Based on this new science, ways of further improvement of the CdTe solar cells are proposed. The chapter also briefly presents the latest experimental observations proving these suggestions.

4.2 The Conventional Model for a Glass/Conducting Glass/CdS/CdTe/Metal Solar Cell

The main subject of this chapter is the CdTe-based thin-film solar cell, which consists of two semiconducting layers. The wide-bandgap n-type CdS (E_g = 2.42 eV) layer serves as the window material, and the narrow-bandgap CdTe (E_g = 1.45 eV) layer is used as the absorber material. If the CdTe layer is p-type, then the active junction is a simple p-n-type hetero-junction and the required internal electric field within the device is provided by this interface. To date, various methods have been used to grow CdS and CdTe and fabricate this solar cell device. A genuine p-n junction device could have a typical structure of metal-1/n-CdS/p-CdTe/metal-2, providing two ohmic contacts for the collection of photo-generated current, as shown in Fig. 4.1. Metal-1 serves as the ohmic contact to

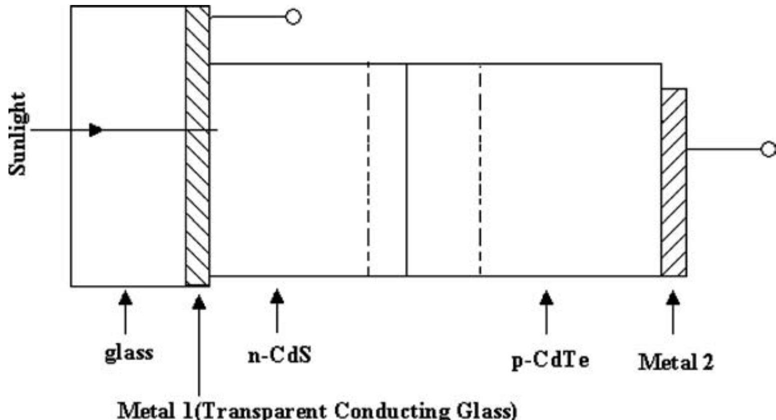

Figure 4.1 A shematic diagram of the glass/conducting glass (metal-1)/CdS/CdTe/metal-2 device structure according to the simple p-n junction model.

the n-CdS layer, and suitable electrical contacts such as Au, Cu/Au, Cu/Ni or Ni serve as the ohmic contacts to the p-type CdTe layer. The energy band diagram of such a device is shown in Fig. 4.2.

A large number of research groups has worked on glass/conducting glass (CG)/CdS/CdTe/metal structures, depositing low-cost CdS and CdTe semiconducting layers, on glass/CG substrates. The CG used is usually indium tin oxide (ITO) or fluorine-doped tin oxide (FTO) with metallic conduction and over 90% light transparency. In principle, any transparent conducting layer with high transparency of light and low sheet resistance for electrical conduction can be used in these devices. The CdS layer used is always n-type, and various growth methods such as chemical bath deposition (CBD), electrodeposition, spray pyrolysis, and vacuum evaporation have been used to produce this window layer. The thickness of the CdS window layer varies from 80 nm to a few microns according to the work reported in the literature. The absorber layer, CdTe, has also been produced using a variety of methods such as the close-space sublimation technique (CSST), electrodeposition, and screen printing. The thickness of the CdTe layer varies in the range 1.5–5.0 μm, and a typical device may contain a 0.1 μm CdS and ~2.0 μm CdTe layers. The fabrication process for the complete solar cell also includes chemical treatment,

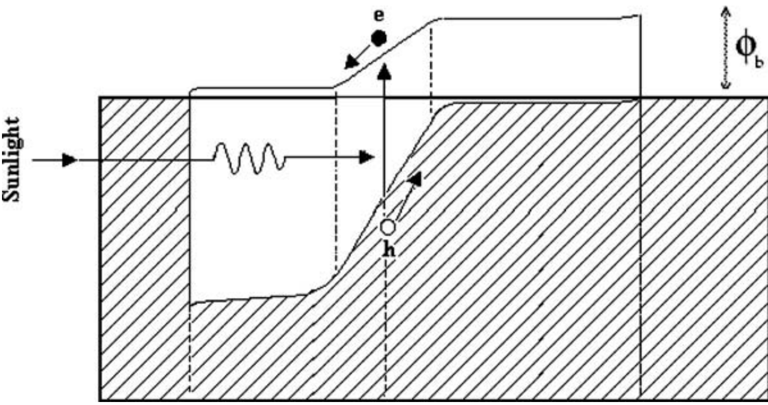

Figure 4.2 An energy band diagram of the glass/CG(metal-1)/CdS/CdTe/metal-2 solar cell based on the p-n junction model. Note the ohmic contact required to the p-type CdTe/metal interface according to this model (not to scale).

post-deposition heat treatment, chemical etching, and metallisation. The chemical treatment of the CdTe layer with $CdCl_2$ followed by heat treatment in air at 350–450°C for ~20 minutes are crucial steps for obtaining PV activity with high efficiencies. This device was fabricated using electrodeposited CdTe by Basol *et al.* in the early 1980s [5, 6], and the observed PV effect was explained in terms of complete type conversion of the CdTe layer during the annealing in air, forming an active p-n junction at the n-CdS/p-CdTe interface. This original work produced an excellent device with a good scientific explanation to describe its action. Research activities have been carried out, and results were explained to fit with the already accepted p-n junction model. However, the development of this device has been delayed due to lack of proper exploration, independent analysis, and deep understanding. Comprehensive work on metal/CdTe interfaces [7] over the same period led to the emergence of an alternative concept in 2002 [8] to describe the action of this solar cell and to propose new methods of further improving its performance.

4.3 Key Observations That Led to the Formulation of a New Model

This section summarises the key experimental observations which led to the formation of the new device concept for CdS/CdTe solar cells.

4.3.1 *Surface Modification of CdTe*

Previous reports on work on crystalline CdTe have shown that it is possible to modify the stoichiometry of the CdTe surface drastically by chemical etching [9, 10]. Acidic solutions preferentially remove Cd from the CdTe surface, leaving a Te-rich surface, and alkaline solutions preferentially remove Te from the surface, leaving a Cd-rich surface [9, 10]. This was revealed by X-ray photoelectron spectroscopy (XPS), as shown in Fig. 4.3.

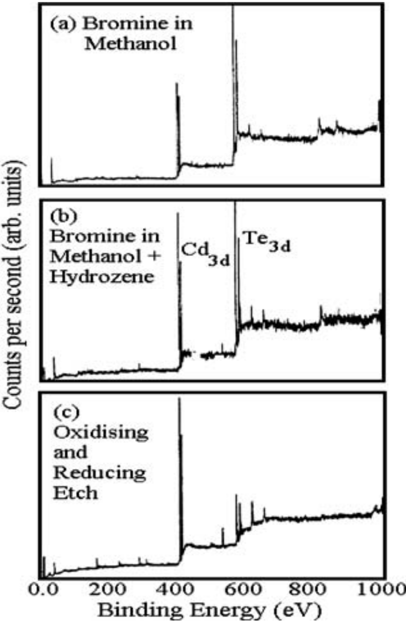

Figure 4.3 XPS spectra showing the possibility of producing (a) Te-rich and (c) Cd-rich CdTe layers by chemical etching in acidic and alkaline solutions, respectively [10].

4.3.2 *Effects of Surface Modification on Defect Levels*

Photoluminescence (PL) experiments have been carried out to investigate the effects of surface modification on defect levels within the bandgap. PL peaks observed from Te-rich (a, b, c) and Cd-rich (d, e, f) CdTe surfaces as a function of photon energy at temperatures of 4 K are shown in panel (a) of Fig. 4.4 [11]. Peak positions have been converted to room temperature values using -5×10^{-4} eVK^{-1} for the rate of change of the CdTe bandgap with temperature [12]. These results indicate the existence of 0.72 eV level for Te-rich surfaces and enhancement of 0.97 eV and 1.24 eV for Cd-rich surfaces at room temperature. Possible electron transitions during PL measurements are shown in panel (b).

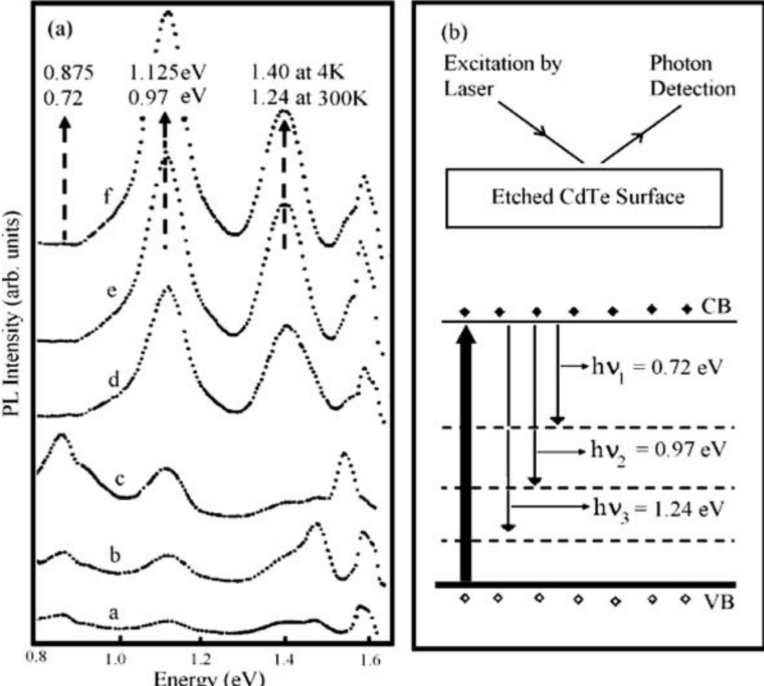

Figure 4.4 (a) PL spectra observed for Te-rich (a, b, c) and Cd-rich (d, e, f) surfaces and (b) a schematic diagram of the corresponding electron transitions [11].

4.3.3 *Effects of Defect Levels on Electronic Devices*

The investigation of metal/n-CdTe interfaces fabricated on chemically etched bulk CdTe surfaces revealed that the Fermi level tends to pin at 0.72 eV on Te-rich surfaces and at ~0.96 eV on Cd-rich surfaces. Detailed metal contacts on vacuum-cleaved, chemically etched, and air-cleaved surfaces revealed that there are at least five different Fermi-level pinning positions [7, 13, 14]. Three sets of I-V curves showing three different pinning positions are shown in Fig. 4.5 [7, 13, 14]. These have been observed for the same metal gold (Au) or antimony (Sb) on the same n-CdTe bulk crystals with only the surface preparation method being different.

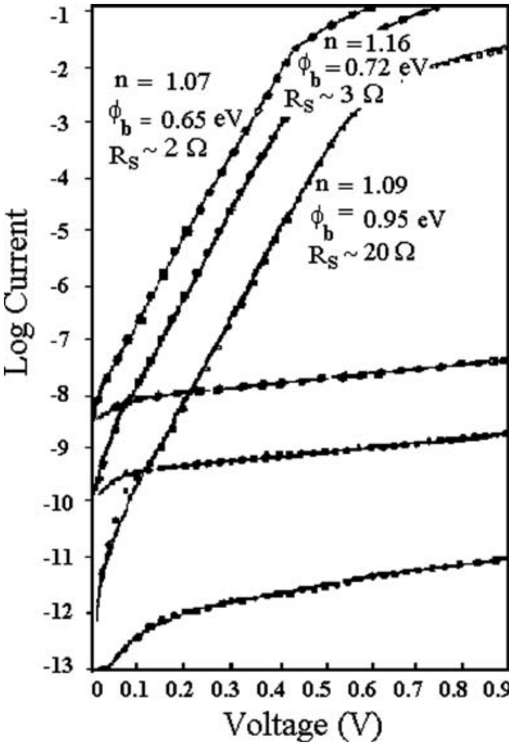

Figure 4.5 Three different sets of I-V curves observed for metal/n-CdTe bulk crystals indicating Fermi-level pinning at different positions [10].

Comprehensive work on electrical contacts to n-CdTe bulk crystals with over 20 different contacting materials show that Fermi-level pinning is a strong mechanism in these interfaces and determined by the history of material growth and the nature of surface [7]. Chemical etching could modify this situation to a certain extent. This work has also shown that Sb produced the noise-free and most stable electrical contacts to form Schottky barriers to n-CdTe surfaces. Furthermore, the best I-V curves with the highest RF ($\sim 10^9$) and the lowest ideality factor (n) are observed when the CdTe surfaces are produced with Cd richness [10] and the metal contacts are formed with Sb.

All the experimentally observed Fermi-level pinning positions, as measured by different techniques, are summarised in Table 4.1 and schematically shown in Fig. 4.6. The agreement of the locations determined by four different techniques for defects in CdTe is conclusive and impressive.

Table 4.1 Discrete Fermi-level pinning positions measured using I-V and ballistic electron emission microscopy (BEEM) techniques and deep levels observed using PL and deep-level transient spectroscopy (DLTS) techniques for n-CdTe bulk crystals [7]

$(\phi_b)_{IV}$ (eV)	PL ($E_c - E_t$)eV	DLTS ($E_c - E_t$) eV	BEEM (ϕ_b)eV
0.40 ± 0.04	—	0.42 ± 0.03	—
0.65 ± 0.02	—	0.65 ± 0.03	—
0.73 ± 0.02	0.715 ± 0.005	0.74 ± 0.03	—
0.96 ± 0.04	0.965 ± 0.005	0.95 ± 0.03	0.96
1.18 ± 0.02	1.240 ± 0.005	1.18 ± 0.04	—

4.3.4 *Similar Observations on Thin-Film CdS/CdTe Solar Cells*

Current-voltage (I-V) measurements of a large number of thin-film solar cells (glass/CG/CdS/CdTe/metal) fabricated using electrodeposited CdTe showed discrete barrier heights in agreement with results obtained for bulk n-CdTe/metal Schottky diodes. These results are summarised in Fig. 4.7(a). The V_{oc} values measured under illumination conditions also follow similar discrete values, indicating Fermi-level pinning at different levels for different batches

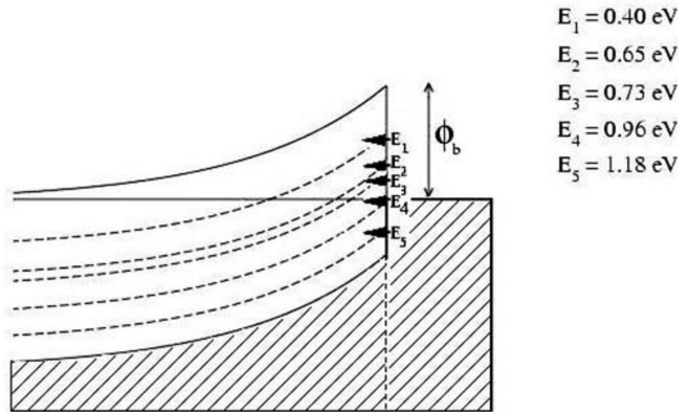

Figure 4.6 Experimentally observed possible Fermi-level pinning positions when a metal is evaporated on to n-type CdTe bulk crystals [7, 15].

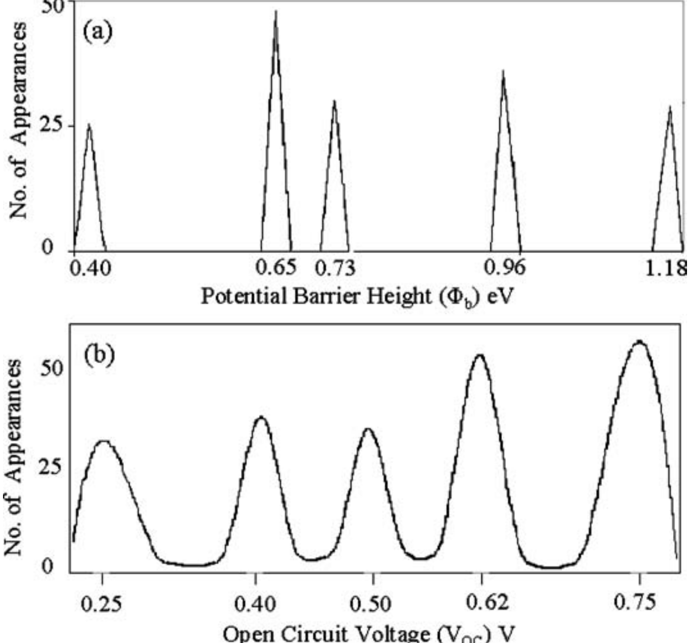

Figure 4.7 (a) Discrete barrier heights and (b) different open circuit voltage values observed for glass/CG/CdS/CdTe/metal thin-film solar cells fabricated with electrodeposited CdTe [8].

of processing — see Fig. 4.7(b). The observation of very similar behaviour in Schottky barrier formation at metal contacts to bulk crystal CdTe and thin-film CdTe layers is a unique property of CdTe [8].

4.4 New Concept for CdS/CdTe Solar Cell

This new device concept follows the work on metal contacts to II-VI semiconductors, as reported in a review article in 1998 [7] and as summarised in section 4.3. As a result of a large body of information, it has been shown that a Schottky barrier forms at the metal/n-CdTe interface, as shown in Fig. 4.6. This work was carried out on various n-type bulk CdTe materials, and the Schottky barrier formation is found to be governed by Fermi-level pinning at one of the five possible discrete levels. These experimentally identified defect levels are situated in the bandgap at 0.40 ± 0.04, 0.65 ± 0.02, 0.73 ± 0.02, 0.96 ± 0.04, and 1.18 ± 0.02 eV below the conduction band minimum. Depending on the growth history of the material, fabrication process, and the metal contact used, the Fermi-level pinning will take place at one of the above five levels. The high density of these local defect states can be found in the top surface layer with a thickness of a few 100 Å, and some of these defects coincide with the native defects found in the bulk material. The thickness of this modified surface layer depends on the surface treatment and etching prior to metallisation. Although this work was carried out in the past on bulk CdTe crystals, the subsequent work on electrodeposited CdTe thin layers has produced an identical picture, as described in section 4.3. It is an astonishing property of CdTe that the same picture emerges from most of the published work in the literature, irrespective of the growth method used for the production of CdTe layers. The above behaviour was observed for solar cells based on electrodeposited CdTe layers, showing efficiencies above 10% for lab-scale devices. Therefore, the following descriptions are relevant only for best devices fabricated out of the CdS/CdTe material system.

When a glass/CG/CdS/CdTe/metal structure is fabricated using CBD-CdS and electrodeposited CdTe (ED-CdTe) the structure and

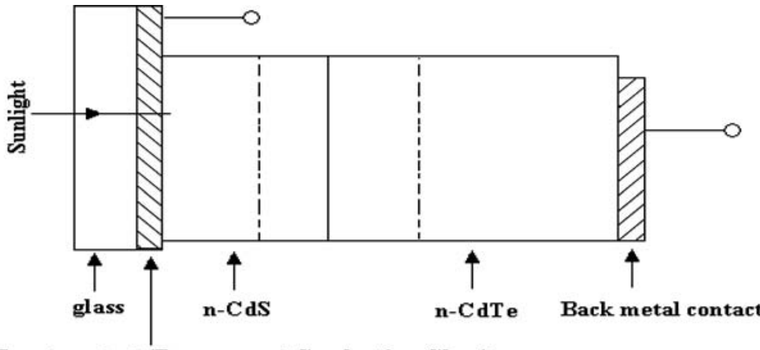

Figure 4.8 A schematic diagram of the glass/CG(metal-1)/CdS/CdTe/metal-2 device structure according to the new understanding (not to scale).

the energy band diagram of the device according to the new understanding takes the form shown in Figs. 4.8 and 4.9, respectively. In these devices, the CdS layer is n-type and usually provides a better substrate than the conducting glass for growth of high-quality CdTe material. During the annealing process, the intermixing of CdS and CdTe takes place, forming CdS_xTe_{1-x} ternary compounds, creating a graded bandgap interface at the hetero-junction. Chemical treatments and the annealing process improve the crystallinity of the semiconducting layers, form larger grains, remove unwanted defects in the material, passivate grain boundaries, and bring the doping concentrations to moderate values in the range mid-10^{14} to mid-10^{17} cm^{-3}. The bulk of the CdTe layer remains n-type during processing, and the outermost layer contains high concentrations of defects responsible for Fermi-level pinning at one of the five experimentally identified levels. The thickness of the top surface layer varies in the region of a few 100 Å, depending on the processing steps such as the heat treatment and etching procedure. If the Fermi level is pinned close to the valence band, at 0.96 ± 0.04 or 1.18 ± 0.02 eV below the conduction band minimum, a large Schottky barrier is formed at the metal/CdTe interface, creating the required band bending across the device for PV activity. Then, the top surface layer of the CdTe material can be considered a p-type layer since the Fermi level is close to the valence band maximum.

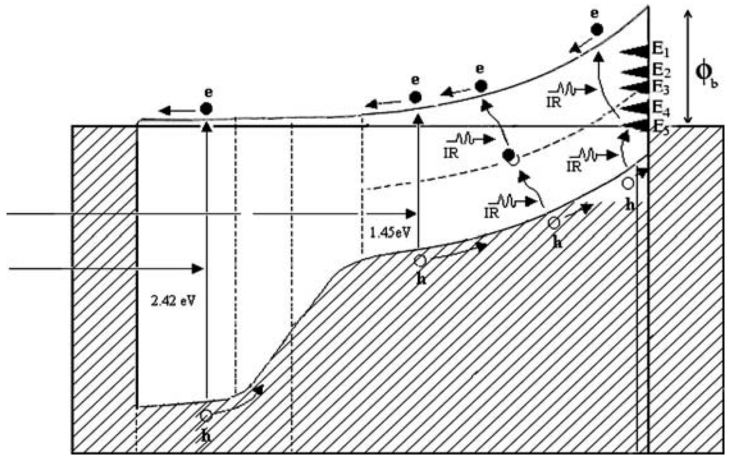

Figure 4.9 An energy band diagram of an n-CdS/n-CdTe hetero-junction together with a large Schottky barrier at the back metal contact [8].

The final device can be completely or partially depleted, depending on the doping concentration achieved for the CdTe layer during growth and subsequent processing. As the energy band diagram in Fig. 4.9 indicates, the internal electric fields near the hetero-junction and the metal/CdTe interface add up, and this becomes a tandem solar cell. If there is good alloying at the CdS/CdTe interface during the annealing process, the device structure is effectively a multi-layer graded bandgap tandem solar cell capable of absorbing a major part of the solar spectrum.

This new model has been formulated mainly using experimental evidence collected by the author over a period of two decades and valid only for high-efficiency CdTe solar cells. The possible band discontinuities and energy spike at the hetero-junction have been neglected for two main reasons. The first reason is the negligible effect of the spike at the hetero-junction when strong band bending is present in the device structure. The second reason is that the intermixing of materials used (CdS/CdTe) in the device structure removes any energy spike at the boundary and produces gradual changes in bandgaps of intermediate phases. The presence of $CdS_xTe_{(1-x)}$ alloys in the device structure has been shown experimentally using photoluminescence and electroluminescense

by Potter *et al.* in 2000 [16] and also by X-ray diffraction and energy dispersive X-ray spectroscopy studies by Terheggen *et al.* [17] in 2001. Fritsche and co-workers [18, 19] reported, in 2001, a comprehensive and systematic study of the band off-sets at hetero-junctions involved in this device. Their findings using photoemission experiments are similar to the band diagram proposed in this model excepting the most crucial Fermi-level pinning situation at the n-CdTe/metal interface.

Under optimum conditions, such a device structure may produce large currents, in excess of the theoretically predicted maximum current density of $\sim$25 mA/cm^2 (Loferski, 1956; M'baye, 1980) for a p-n junction solar cell based on a single bandgap of CdTe [20, 21]. In addition, this solar cell structure benefits from the impurity PV effect creating e-h pairs by making use of defect levels within the bulk of the CdTe and closer to the CdTe/metal interface. Photons with energy less than the bandgap (1.45 eV) are, therefore, able to create e-h pairs, as shown in Fig. 4.9. In this case, since there is a strong electric field for charge carrier separation within the device, R&G centres are favourably used to create more charge carriers to produce a higher current in the external circuit. In fact, the ladder of defect levels (E_1–E_5) at the back metal/CdTe interface creates useful charge carriers using low-energy IR photons through the process of multi-step charge carrier promotion. According to this new model, CG forms an ohmic contact to n-CdS and the back metal contact forms a large Schottky barrier at the metal/CdTe interface. In contrast, the p-n junction model requires a completely opposite formation of an ohmic contact at the back metal/CdTe interface.

4.5 Description of Experimental Results Using the Two Models

It is now worth comparing the two device concepts, as shown in Fig. 4.10, to describe and understand experimentally observed results from different techniques. This will allow the identification of key information necessary to recognise the need of a new concept for deep understanding and, hence, further development of this device.

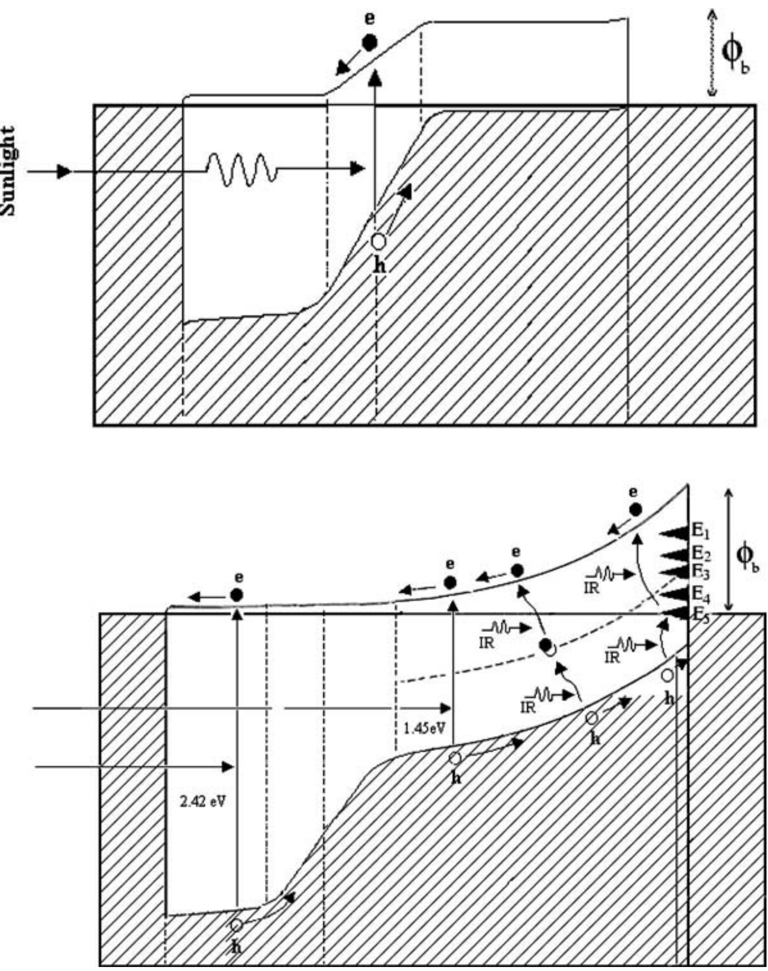

Figure 4.10 The energy band diagrams of the previous concept and the new concept for description and comparison of experimental results.

4.5.1 *Current-Voltage (I-V) Characteristics*

When sunlight enters through the glass/CG side, the photo-generated charge carriers are created within the semiconducting layers, separated by the internal electric field, and collected to create an electric current in the external circuit. In both models, electrons flow towards the conducting glass and holes flow towards the back

metal contact, making the CG layer negative and the metal contact positive in polarity. Both models produce similar polarity, making it unnecessary to think differently from the already assumed p-n junction model. Similar I-V characteristics with rectifying properties and PV activities can be produced by both device structures. The only difference will be the higher performance from the second device structure due to the combination of two supporting rectifying junctions in one device and the additional contributions from the impurity PV effect.

4.5.2 *Capacitance-Voltage (C-V) Characteristics*

According to both models, C-V measurements are possible due to the presence of at least one active (rectifying) interface within each device structure and, hence, a depletion region. If the device is fully depleted due to low doping concentrations of CdTe, in the region of 10^{15} cm^{-3} or below, capacitance values remain almost unchanged with the applied bias voltage and approximately equal to the geometric capacitance of the structure. If the doping concentration is such that the depletion region covers only a part of the CdTe layer thickness, then the capacitance varies according to the applied bias voltage providing linear $1/C^2$ versus bias voltage (Schottky-Mott) plots and the estimated doping concentration lies in the range 10^{16}–10^{17} cm^{-3}. There are numerous examples of such C-V measurements in the literature, and these demonstrate this behaviour giving doping concentrations in the range 10^{15}–10^{17} cm^{-3}. The works reported in publications by Raychaudhuri in 1987 [22], Chu *et al.* in 1988 [12], Morris *et al.* in 1991 [23], and Das *et al.* in 1993 [24, 25] are good examples of devices with efficiencies close to 10%. Similar C-V observations could arise from both types of devices, making it more difficult to distinguish between the two models applicable to this system.

4.5.3 *Electron Beam–Induced Current Measurements*

There are various reports in the literature giving electron beam–induced current (EBIC) results for such devices with contradicting conclusions (Mitchell *et al.*, 1977 [26], Nakayama *et al.*, 1980 [27],

Bhattacharya *et al.*, 1985 [28], and Galloway *et al.*, 1995 [29]). This method creates a peak of EBIC at the junction area where the internal electric field is maximum. However, previous reports have shown peaks appearing at the CdS/CdTe interface, in the middle region of the CdTe layer, and at the metal/CdTe interface and, therefore, provide inconclusive EBIC results. In fact, if the device is fully depleted, the EBIC peak could appear at any place where the material quality is high and, therefore, the charge carrier collection is more efficient. The EBIC results reported in the past could be explained using both models for this device structure.

4.5.4 *Observation of Discrete Barrier Heights and V_{oc} Values*

Figure 4.7 summarised the experimentally observed potential barrier height (ϕ_b) values and discrete set of V_{oc} values for thin-film CdS/CdTe solar cells. These observations arouse curiosity about the device structure. If the device is a simple p-n junction, it provides only one ϕ_b depending on the bandgaps of the two materials. Observations of five different barrier heights and discrete sets of V_{oc} values for different batches of the same solar cell structure provide the main reason to move away from the p-n junction model. Fermi-level pinning positions observed at CdTe/metal interfaces (as shown in Fig. 4.6), the exact match between these Fermi-level positions with experimentally measured ϕ_b values, and the presence of five different sets of V_{oc} values strongly supported the formation of new model for this device structure.

4.5.5 *A Thin-Film CdTe Solar Cell Device Without a CdS Layer*

There exists one report in the literature on the comparison of CdTe solar cells with and without a CdS layer. Das and Morris [24, 25] established the electrodeposition of CdTe and fabricated thin-film solar cells under similar conditions, one set with CdS and the other set without CdS. This work produced solar cells with efficiencies around 10%, but the device without a CdS layer showed comparatively better performance. These researchers must have had substrate preparation conditions right for CdTe to grow on CG

rather than CG/CdS surfaces. This information is vital to recognise that the rectification property required for the PV effect is not due to the CdS/CdTe hetero-junction but due to the large Schottky barrier formed at the back CdTe/metal interface. Various other reports in the literature and authors' recent works highlight that better performance is achieved with thinner CdS layers, in the order of 50 nm [30]. In fact, the new understanding is that the CdS layer provides a better nucleation surface for CdTe to grow but the layer is partially or completely consumed at this interface by the post-deposition heat treatment of the device. Such a thin layer of 50 nm of CdS will not survive in the presence of the 1500 nm (1.5 μm) thick CdTe layer, to form an identifiable semiconductor, and hence provide a 2.42 eV bandgap to form a clean p-n junction. The interface chemistry taking place during about 5 hours of electrodeposition of CdTe and post-growth heat treatment at 450°C for 20 minutes will form mixed phases, $CdS_xTe_{(1-x)}$ at this interface. However, if the CdS layer is thick enough, this will form a graded bandgap interface with bandgaps varying from 2.42 eV (CdS) to 1.45 eV (CdTe) due to the partial consumption of the CdS layer in the middle.

4.5.6 *Results From Electrical Contacting Work*

Since the Schottky barrier at the metal/CdTe interface is determined by Fermi-level pining, almost any electrical contact shows the PV activity with different efficiencies for this device, provided the electrical contact used does not completely destroy the p-layer or the Fermi-level pinning effect on the surface. For example, metals such as Cu, Sb, and As, p-type dopants of CdTe, help to keep the Fermi level close to the valence band and, hence, produce low-resistance contacts. This will provide good results for freshly made devices, but with aging, metals like Cu diffuse into the n-type CdTe region (i.e., beyond the surface p-layer) and form a highly resistive layer due to self-compensation. Therefore, the device will rapidly deteriorate, showing an increased contact resistance. However, a contact containing a small amount of Cu will reduce the contact resistance due to p^+ doping of the surface p-layer without getting into the n-CdTe region. For this reason, Cu/Ni or Cu/Au contacts with less than ~5% Cu should act as low-resistance electrical

contacts. If the device is a simple p-n junction, Cu should always produce a good ohmic contact to p-CdTe and should improve ohmic behaviour with aging, due to in-diffusion of this p-type dopant, instead of forming highly resistive contacts with aging. These experimental observations provide supporting evidence for the proposed alternative model, and the p-n junction model fails to explain the results. Because of the p-type doping of Sb and the low diffusivity through the material due to its high chemical bonding, Sb-containing electrical contacts should form superior and stable contacts to this solar cell. This has been demonstrated for Sb/n-CdTe Schottky contacts, as discussed in section 4.3.3.

If group III elements, such as indium or aluminium, are used as the contact metal, PV activity may still be observed with a large series resistance and, hence, with a very small fill factor (FF). This is due to the compensation effect introduced by n-type dopants (In or Al) in the p-type CdTe surface layer. A series resistance of 2 MΩ has been observed for indium contacts, when copper-containing contacts have shown only ~50 Ω series resistance for 2 mm diameter devices [8, 30]. In many situations, if the p-type surface layer is very thin and the interactions of indium and aluminium are considerable during the metallisation step, the metal contacts completely consume the surface p-layer, reaching the n-type CdTe, producing an ohmic contact. In these situations, there is no PV activity observed for the device and the I-V curves show nearly ohmic behaviour with low series resistance. These observations provide paramount information to move away from the p-n junction model and towards the proposed new device concept. This nearly ohmic behaviour also indicates the weak rectifying property of the n-CdS/n-CdTe hetero-junction.

4.5.7 *Doping of CdS and CdTe Layers*

The main improvement necessary in this type of device is the reduction of series resistance to increase the FF. Very thoughtful experiments have been carried out by some groups, on the basis of the assumed p-n junction model in the past, and reported by Dennison in 1994 [31]. A typical device contains about 1.5 μm

thick CdTe and a negligibly thin (50–100 nm) CdS layer grown on the CG substrate. Therefore, the main body of this device contains 1500 nm of CdTe, and if this material is assumed to be p-type, the most sensible doping is with a p-type dopant in CdTe to reduce the resistance. All three Na, Cu, and Ag are well established p-dopants in CdTe, as well documented in de Nobel's thesis [32] and by Zanio in 1978 [33], and these elements have been added with fine control to the CdTe layers. The most unexpected results were observed with an increased shunt resistance, increased series resistance of the diodes, and, hence, a drastic reduction of the efficiency mainly due to loss in the FF. This clearly shows that the main body of n-type CdTe material becomes resistive due to self-compensation during doping with p-type dopants such as Na, Cu, and Ag. This experimental evidence confirms the new model proposed for this device and cannot be explained using the assumed p-n junction model.

The positive effects on device performance of $CdCl_2$ treatment [34] of both CdS and CdTe layers have been puzzling researchers during the past few decades. In the $CdCl_2$ treatment, according to the new model, chlorine clearly helps the n-type doping of both semiconductor layers, reducing the series resistance and, hence, improving the FF drastically. This treatment also helps to keep the CdTe surface rich in Cd, which is necessary for producing high-quality Schottky barriers at metal/n-CdTe interfaces (see section 4.3.3). There may also be other benefits, such as the cementing effect of chlorine to form larger grains, reducing grain boundaries, but there are contradictory reports indicating substantial improvement of efficiency without any observable grain size improvements [18, 19]. There are also reports on the basis of PL measurements that halogens are effective in reducing mid-gap defect levels in CdTe. All previous reports did not even consider the possibility of n-type doping of the CdTe layer by chlorine since all the explanations are based on the already accepted p-n junction device model. It should be noted that chlorine (a halogen) is a well established and reliable n-type dopant for CdTe material [32, 33]. This most crucial $CdCl_2$ treatment needed for drastic device improvement, therefore, provides strong supporting evidence for the new model.

4.5.8 *Further Experimental Evidence to Confirm the True Structure of the Device*

The observed results and interpretations presented in the above sections provide strong supporting evidence for the proposed new model based on Fermi-level pinning at metal/n-CdTe interface. The following experiments have been carried out to further confirm the new device structure [8].

Following the usual procedure to fabricate the device structure, Au contacts and In/Ga contacts were made side by side on the same sample, as shown in Fig. 4.11. The In/Ga contacts were made by painting In/Ga eutectic at room temperature and then annealing using a fine soldering iron tip to consume the top surface layer and, hence, to form a good ohmic contact between In/Ga and the CdTe layer. Various contact combinations, as labelled in Fig. 4.11, were measured, and the observations and conclusions are summarised in Table 4.2.

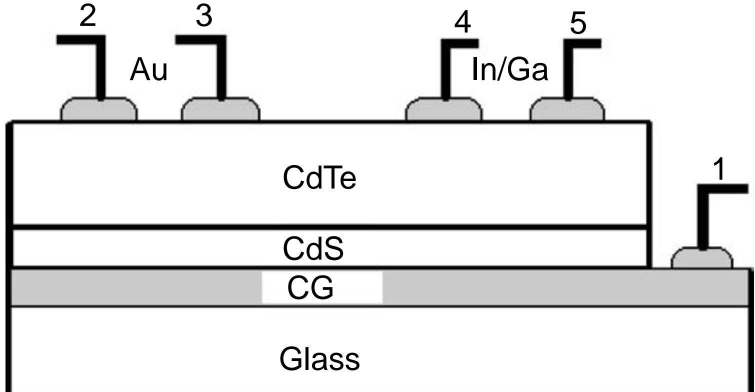

Figure 4.11 The electrical contacts used to identify the location of the rectifying interface. Au and In/Ga contacts are used side by side to measure I-V curves. The measurement results and conclusions drawn are summarised in Table 4.2. The CdS/CdTe device structures used to perform this experiment produced conversion efficiencies of approximately 10%.

The above measurements confirm the existence of a large Schottky barrier at the Au/CdTe interface and the non-existence of a considerable rectifying contact at the n-CdS/n-CdTe hetero-junction.

Table 4.2 The summary of I-V measurements carried out between different electrical contacts made on the device, as shown in Fig. 4.11, and the conclusions arising from these measurements. The CG/CdS/CdTe/Au device structures used to perform this experiment produced conversion efficiencies of approximately 10%

Two Contacts Measured	Observations	Remarks and Conclusions
1. Measurements between Au and CG (1 and 2) and (1 and 3)	Efficiency is ~10%. Rectifying contacts with reverse current of $\sim10^{-7}$ A. Series resistance is ~100 Ω.	There are good solar cells between Au and CG contacts.
2. Measurements between two Au contacts (2 and 3)	Efficiency is ~0%, and current in both directions are in the order of 10^{-7} A.	Two Schottky diodes are back to back. Therefore, the current measured is the reverse current of one of the diodes and there is no PV activity from this combination.
3. Measurements between In/Ga and CG (1 and 4) and (1 and 5)	Nil or little PV activity and ohmic currents are observed with series resistance of ~80 Ω.	Annealed In/Ga contacts consume p-surface layer and make good ohmic contacts to the n-CdTe layer. There is no considerable rectification at n-CdS/n-CdTe interface, and, therefore, PV activity is minimal.
4. Measurements between two In/Ga contacts (4 and 5)	No PV activity and good ohmic currents with series resistance of ~30 Ω are observed.	In/Ga make ohmic contacts to n-CdTe, and, therefore, conduction is through the CdTe layer. There is no rectifying interface between the two contacts.
5. Measurements between Au and In/Ga (2 and 4) and (3 and 5)	Efficiency is ~10%. Rectifying contacts with reverse current $\sim10^{-7}$ A. Series resistance is ~40 Ω.	In/Ga provide ohmic contacts to n-CdTe, and the Au contact provides rectifying properties. Therefore, this combination represents a good solar cell only with the Schottky barrier at the Au/CdTe interface without the involvement of the CdS layer.

It is also noteworthy that Das and Morris, in 1993, produced a better solar cell of 9.8% efficiency for the ITO/SnO_2/CdTe/metal structure without the CdS layer than a solar cell of 8.8% efficiency for the ITO/SnO_2/CdS/CdTe/metal device with the CdS layer [24, 25]. This clearly indicates that the rectifying contact required for PV activity is at the metal/CdTe interface rather than at the CdS/CdTe hetero-junction. This is equivalent to the situation described by case number 5 in Table 4.2.

A large body of subsequent measurements on glass/CG/CdS/CdTe/metal thin film solar cell structures fabricated using electrodeposited materials confirmed the Fermi-level pinning at discrete levels — Fig. 4.7(a). It is interesting to note exactly the same barrier heights observed for electrodeposited CdTe thin layers as observed for metal contacts on bulk n-type CdTe (see Fig. 4.6). This indicates that the defect levels (E_1–E_5) responsible are arriving from native defects of CdTe and do not strongly depend on the method of growth. These different barrier heights appear for different batches of fabrication, and their respective V_{oc} values also tend to produce values in discrete nature, as shown in Fig. 4.7(b). The V_{oc} values follow respective barrier heights since this parameter is a function of the barrier height (Eq. 1.16). In order to produce high efficiency solar cells, the Fermi level should be pinned at either 0.96 ± 0.04 or 1.18 ± 0.02 eV level below the conduction band minimum. The latter value is the most preferred value for best devices.

4.6 Predictions for Further Development of CdS/CdTe Solar Cells and Latest Observations

The experimental results available to date enabled the formulation of this alternative model; hence, the following main steps should allow further improvement of this solar cell structure to achieve higher efficiencies.

4.6.1 *Doping of Window and Absorber Materials with n-Dopants*

The use of glass/CG substrates with lowest sheet resistance and the selection of a suitable n-type window material with required

qualities will be a good starting point. Better crystallinity, lowest possible number of defects, and the doping concentration close to 10^{16} cm^{-3} will be desirable for the window material. In the case of n-CdS, the doping of the material with group III elements or group VII elements will enhance the electrical conductivity of the films. However, the introduction of some of these elements may disrupt the crystallinity, increasing the number of defects, and reducing the mobility of charge carriers and, hence, reducing the required electrical conductivity. Obtaining the optimum electrical conductivity is a challenging task, but every positive step will contribute to the enhancement of the device performance. The $CdCl_2$ treatment of the CdS layer has already shown the positive effects of doping with chlorine. Alternative window materials such as ZnS, InS, and ZnO should be explored. Any window layer which provides a better substrate for CdTe to form larger grains, especially in the forms of columns perpendicular to the substrate, will enhance the device efficiency.

The absorber layer (CdTe), of the order of $\sim$2 μm thickness, should have the desired semiconducting qualities such as better crystallinity, larger grains, passivated grain boundaries, minimum possible R&G centres, and the lowest possible background impurities. All these desired properties will increase the charge carrier mobility, enhancing the electrical conduction. The material layer should retain n-type electrical conduction, and, hence, the ideal dopants will be group III or group VII elements. The achievement of doping concentrations in the desired region of $\sim 5 \times 10^{14}$ to 5×10^{16} cm^{-3} will be ideal for this device structure. Many factors contribute to this ultimate doping concentration and, hence, to the achievement of the optimum electrical conductivity for this layer. This requires systematic experimentation on materials growth, impurity identification and removal or passivation, doping, and processing steps, including heat treatment. The processing steps, including chemical treatments with cadmium halide solutions, heat treatment in air, and the wet-etching process should produce a CdTe layer with optimum n-type properties together with a p-type surface layer in the order of a few 100 Å, to achieve the Fermi-level pinning close to the valence band maximum.

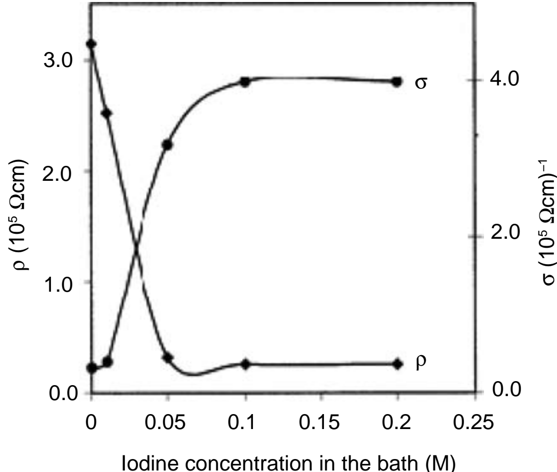

Figure 4.12 The improvement of electrical conductivity (σ) of CdTe layers as a function of I_2 concentration in an electrodeposition bath [35].

In order to test n doping of CdTe, CdS/CdTe device structures were fabricated using CBD-CdS and ED-CdTe using non-aqueous electrolytic baths [35]. By growing CdTe at an elevated temperature of $\sim$170°C, layers with larger grains were produced to achieve high material qualities. The CdTe was doped with varying amounts of I_2, and the variation of electrical conductivity (resistivity) was investigated. Figure 4.12 shows the expected increase in electrical conductivity, proving the n doping of I_2 in CdTe.

The completed glass/CG/CdS/CdTe/Au devices were characterised using I-V and C-V techniques to study the solar cell parameters. The I-V curves measured under dark conditions are shown in Fig. 4.13(a) in the log-linear scale. The rectification factors as defined by I_F/I_R at 1.0 V for best devices show over 4 orders of magnitude. It should be noted that to achieve over 12% efficiencies from this system, only 3 orders of magnitude rectification factor is sufficient [30]. The barrier heights extracted from the diodes which show ideality factors less than 1.40 provide ϕ_b values close to 1.18 eV, which is the most desired Fermi-level pinning position closest to the valence band maximum. Both the n and the ϕ_b

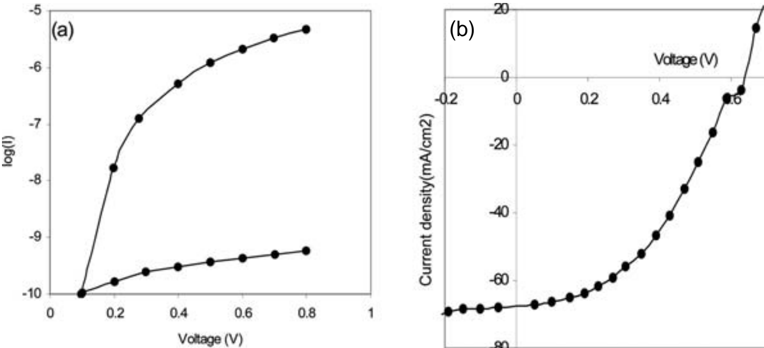

Figure 4.13 The I-V curves obtained under (a) dark and (b) illuminated (air-mass 1.5, or AM1.5) conditions for improved devices with iodine doping. The barrier height of 1.18 eV due to the Fermi-level pinning at the most desired E_5 defect level and the high J_{sc} (over 60 mA/cm^2) have been observed. The kinks appearing on I-V curves are due to the existence of multi-defect levels and described in details in chapter 9.

values were evaluated using the standard method established for the characterisation of Schottky contacts [36].

A typical linear-linear I-V curve under AM1.5 illumination for these latest devices is shown in Fig. 4.13(c). The V_{oc} over 600 mV and fill factors in the range (0.50–0.60) are typical values obtained for these devices, but the J_{sc} (over 60 mA/cm^2) is strikingly high. The above parameters produce efficiencies of ~18%, which is above the highest values, 16.5% reported to date [2].

The capacitance of the above structures was measured as a function of applied bias voltage, at a measurement frequency of 1 MHz. The results are shown in Fig. 4.14, and the device capacitance remains unchanged at ~56 pF with the applied bias voltage. It is, therefore, evident that the depletion width of the device structure is greater than the combined thickness of CdS/CdTe layers. In other words, the device structure is fully depleted, and, therefore, the complete semiconductor layers are PV active. The calculated geometrical capacitance of the 2 mm diameter contact is about 80 pF (assuming $\varepsilon_r = 11$ for CdTe and thickness of the device $= 2$ μm) and comparable to the measured value of ~56 pF. Because a constant capacitance of the same order as the geometrical

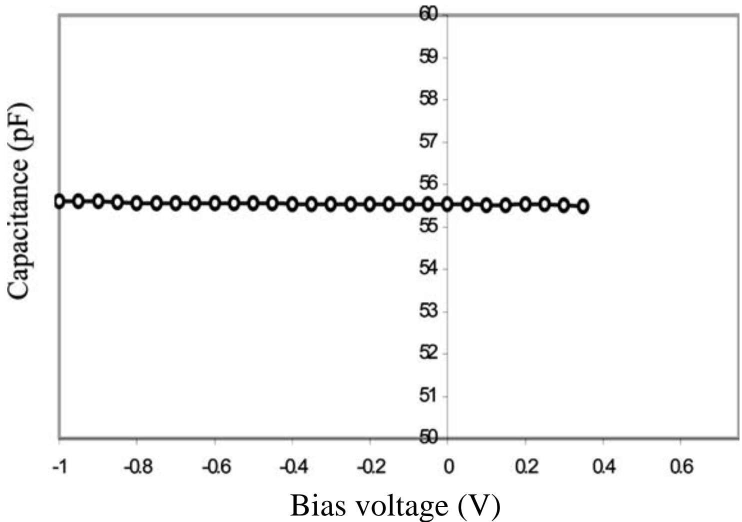

Figure 4.14 The capacitance of glass/CG/CdS/CdTe/Au solar cells observed at 1 MHz measurement frequency as a function of bias voltage. Note the constant capacitance value of ~56 pF due to the presence of a fully depleted solar cell device.

capacitance is observed, further parameters such as ϕ_b or doping concentration cannot be extracted from conventional Schottky-Mott plots. This however, indicates the low doping concentrations (below $\sim 10^{15}$ cm^{-3}) in the CdTe layer, producing a depletion width greater than the complete device thickness [37].

A remarkably high short circuit current density observed for some batches of this solar cell deserves a detailed discussion. The theoretical calculations carried out for p-n junctions of single-bandgap materials show a maximum possible current density of $\sim$25 mA/cm^2 [20, 21]. However, when two or more bandgaps are present in the device structure and two or more active junctions are added to enhance the internal electric field of the device, the situation is completely different. The number of photons absorbed increases rapidly and avoid the device getting heated. This is due to the presence of several bandgap materials reducing thermalisation. Similarly, the separation and collection efficiency increases due to

the enhancement of the internal electric field. In device structures described in this book, the window material has a bandgap of 2.42 eV (CdS) and the absorber material has a bandgap of 1.45 eV (CdTe). In addition, there are varying bandgap material layers consisting of alloys between CdS and CdTe formed during fabrication. As described in chapters 6, 7, and 8, this device structure is capable of creating charge carriers using impurity PV effect. This device structure with optimum conditions is capable of utilising infrared radiation from surroundings to create charge carriers in the device (see chapter 8).

The observation of high J_{sc} is an unusual experimental result that can be observed from time to time. When CdS/CdTe solar cells are fabricated, the J_{sc} value shows a drastic variation. For some batches, these values can be as low as a few mA/cm^2. A majority of the batches produces J_{sc} values in the 20–30 mA/cm^2 range. However, certain batches exhibit J_{sc} values in excess of 40 and 50 mA/cm^2 [8, 35]. For some iodine-doped devices, $\sim$60 mA/cm^2 has been observed, but consistency and reproducibility remain unsolved to date. It should be stressed that this is not due to the variation of light intensity from the solar simulator but genuinely arising from the device itself under some conditions of materials growth and device fabrication. This is a typical behaviour of electronic devices and indicates that these devices can be further developed once the materials issues and device physics have been thoroughly understood.

Independent work by Romeo’s group [38] provides further confirmation of doping with halogens. This group grows CdTe using the close space sublimation and introduces halogen-containing gases — freon (CHF_2Cl) — into the chamber during the growth. This method produces thin-film CdTe, producing small-scale device efficiencies of about 16%. The growth of CdTe at an elevated temperature in the presence of halogen atoms (Cl and F) produces n-type doping and any other benefits provided by halogens in CdTe and, hence, produces high-efficiency devices. These advances by PV researchers confirm the benefits of halogen doping in CdTe. This group also use group-V elements such as Sb and As in order to produce stable back electrical contacts.

4.6.2 *Improvements to Back Contact Using MIS-Type Structures*

For an efficient CdTe-based solar cell device, the Schottky barrier height should be either ~0.96 eV or ~1.18 eV for this system and the latter value is the most beneficial. The formation of lower barriers results in poor performance due to weak band bending and, hence, a weak internal electric field. The selection of a metal contact containing a small amount of p-type dopant such as Cu, Sb, or As further supports the Fermi-level pinning close to the valence band producing an efficient solar cell. Hence, the Cu/Au-, Cu/Ni-, Sb- or As- containing contacts are good candidates to produce highest quality rectifying contacts to this device structure. However, the in-diffusion of a p-type dopant into the n-type CdTe layer should be avoided in order to eliminate the rapid degradation due to the formation of a very resistive electrical contact with aging. When this happens and the efficiency drops down considerably, it should be possible to remove the entire back contact using chemical etching and reproduce the working device again with new metal contacts if there is no damage to the thin-film structure during etching. This procedure should produce high-efficiency devices again, and the preliminary work has indeed confirmed this observation [30].

Introduction of a p-type thin semiconducting layer with a bandgap larger than that of CdTe (e.g., p-ZnTe) or Sb-containing layers such as Sb_2Te_3, will protect the p-type top surface layer from reactions with metal contact, improving both efficiency and durability of the device. Romeo *et al.* in 1999 [39] have indeed shown the positive effects of Sb_2Te_3 incorporation at the back metal contact. A suitable conducting polymer layer with p-type conduction and a bandgap greater than that of CdTe will be an ideal candidate for this purpose to produce inorganic/organic hybrid devices and to increase both efficiency and lifetime of this solar cell.

Another way of improving both performance efficiency and lifetime is by forming an MIS-type contact with an ultra-thin insulating layer [40]. Inorganic compounds such as CaF_2 and SrF_2 or any other insulator will be suitable for this purpose. There is an added value of this approach in the associated pinhole plugging of the device structure, improving the yield of the device fabrication

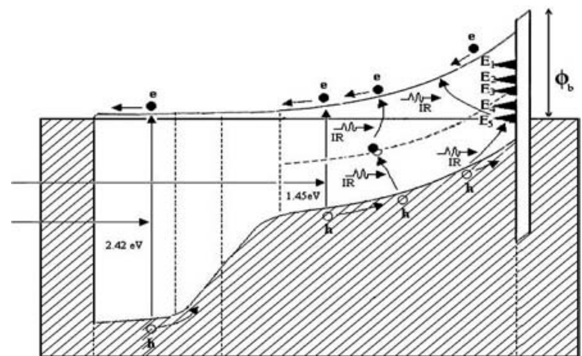

Figure 4.15 An energy band diagram of the glass/CG/CdS/CdTe/CaF_2/Au solar cell with an MIS-type back metal contact [41].

process. To make use of this phenomenon, and to improve the performance of the CdS/CdTe solar cell, preliminary MIS-type electrical contact work has been undertaken using vacuum-evaporated CaF_2 insulating layers [41].

The energy band diagram of such a device showing an improved ϕ_b is shown in Fig. 4.15, and the observed V_{oc} values of MIS structures are shown in Fig. 4.16 together with those of MS structures for comparison. The open circuit voltage has increased for every MIS structure measured, showing more uniform V_{oc} values. In order to keep the material properties similar, the MS and MIS

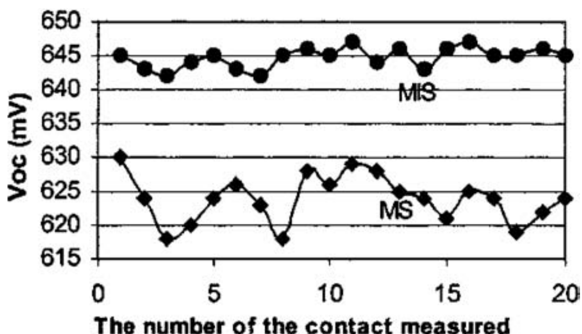

Figure 4.16 Open circuit voltage values measured for glass/CG/CdS/CdTe/Au solar cells with MS- and MIS-type back metal contacts [41].

structures were fabricated side by side, close to each other, on the same sample. These results were obtained for 2 mm diameter circular contacts.

The thickness of the CaF_2 layer was only ~30 Å, as measured using a quartz crystal thickness monitor, so as not to affect J_{sc} and FF. For ultra-thin CaF_2 layers of this type, the overall efficiency is enhanced due to the improvement of V_{oc}, but the efficiency was observed to be reduced as the thickness of CaF_2 increased due to introduction of additional series resistance to the device.

There is an independent report published by Karpov *et al.* in 2003 confirming these MIS-type electrical contacts improving device parameters [42]. This group electrodeposited poly-aniline on the CdTe surface before metalisation and observed a considerable enhancement of the V_{oc} value. The same group also dipped a glass/CG/CdS/CdTe surface in red wine and applied a small DC voltage across the sample with respect to an anode. After this process, the completion of the device was made by drying the surface and metalisation. This procedure enhanced the V_{oc} values considerably by increasing to ~750 mV from their initial values of ~200 mV. In this case, the flavonoid particles (insulating organic particles contained in red wine) have deposited on the CdTe surface, forming an insulating layer. In both these cases, poly-aniline and the flavonoid layer act as insulating layers in these MIS structures.

4.6.3 *A Multi-Layer Graded Bandgap Approach*

The introduction of a third layer with an intermediate energy bandgap will enable the strengthening and smoothing of the slope of the energy band diagram, which is the internal electric field, for the enhancement of the charge carrier collection [8]. A schematic diagram and an energy band diagram of such a device are shown in Figs. 4.17 and 4.18, respectively, and CdSe, with an intermediate bandgap of 1.70 eV, would be an ideal candidate since the element Cd is common to all three semiconductors used. During annealing treatments, the intermixing at hetero-junctions will take place and the device structure will become a graded bandgap multi-layer tandem device with better collection capabilities. These devices will improve at their hetero-junctions with aging and absorb a major

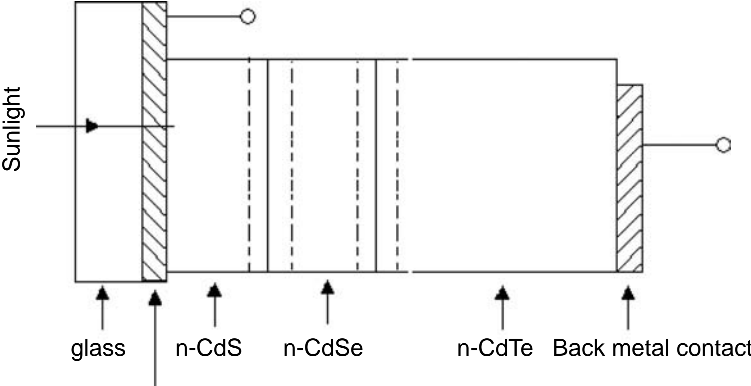

Figure 4.17 A schematic diagram of the glass/CG(metal-1)/n-CdS/n-CdSe/n-CdTe/metal-2 graded bandgap device structure.

part of the solar spectrum due to the effective utilisation of photons at different regions of the device structure. The photons in the IR region with energy less than 1.45 eV are also utilised within the CdTe layer and closer to the back metal contact, as shown in Fig. 4.18, to create photo-generated charge carriers using the impurity PV effect. These carriers will be collected efficiently, with the existing high internal electric field in these thin-film device structures. Theoretical efficiency predicted for this type of devices is high, and therefore the future potential of this device is bright.

4.6.4 *Dealing with Defects*

It has been experimentally shown that there is a drastic effect of defects on Fermi-level pinning at the metal/CdTe interface. Although the exact origins of these defects are not yet clear, some important experimental evidences are emerging. When the surfaces are prepared to have Te richness (Cd deficiencies) the mid-gap defects, 0.65 (E_2) and 0.72 eV (E_3) are dominant. Therefore, Fermi-level pinning produces low Schottky barriers, causing low V_{oc} and the solar cell device performance is poor. Furthermore, the existence of mid-gap R&G centres maximises the recombination process in the device, minimising J_{sc} values of these devices.

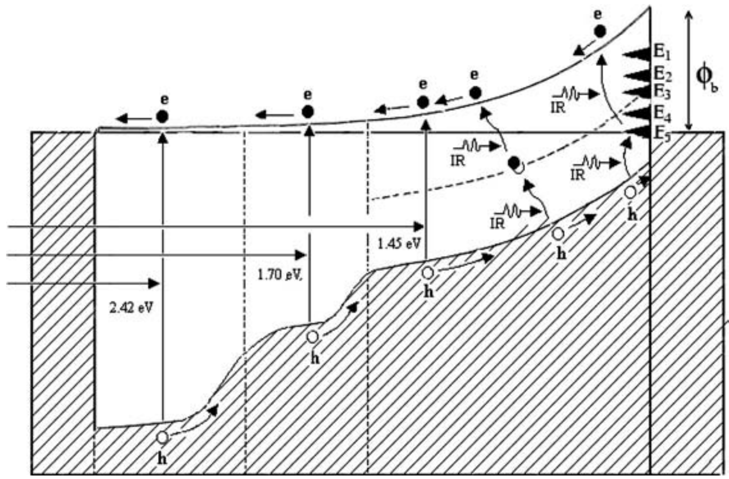

Figure 4.18 An energy band diagram of the three-layer glass/CG/CdS/CdSe/CdTe/metal solar cell with an intermediate CdSe layer. This diagram represents the device in the short circuit mode under illumination [8].

On the other hand, when the CdTe materials and surfaces are prepared with Cd richness (Te deficiencies), the two defect levels 0.96 eV and 1.18 eV are dominating. Therefore, the Fermi level pins at one of these and the best level is $E_5 = 1.18$ eV to produce largest potential barriers and, hence, to produce the highest V_{oc} values. In this case, the mid-gap defect levels (E_2 and E_3) have been minimised (see Fig. 4.4) and hence the recombination process is reduced. Therefore, J_{sc} will be improved.

The effect of defects on both V_{oc} and J_{sc} values is evident from the device fabrication process. This is relevant more often for J_{sc} values observed for different batches. The short circuit current density varies in a wide range, from a few mA/cm^2 to very large values, sometimes exceeding 50 mA/cm^2. This large variation must be due to the detrimental effects of defects in the devices. Large currents appear from time to time, most probably due to the production of devices with minimum defect concentrations. At the present time, the reproducibility of very large J_{sc} values has not been established, but research aims should be to explore reasons and achieve these impressive current densities.

In order to produce high-efficiency solar cells, the CdTe materials should be grown with slight Cd richness, surfaces should be modified to produce Cd richness, and hence the Fermi level should be pinned closer to the valence band maximum at E_4 or E_5. Since there are five defect levels, the reproducibility, stability, and yield of devices are going to suffer unless these defect levels are properly understood and dealt with appropriately.

4.7 Summary

The large body of experimental evidence available in the literature enabled the identification of the necessity of an alternative model to describe and develop the glass/CG/CdS/CdTe/metal solar cell further, beyond the limits of the p-n junction model. This new model explains the device behaviour in terms of a combination of an n-n hetero-junction and a large Schottky barrier at the CdTe/metal interface. The materials growth, chemical, and heat treatments and wet chemical etching provide the right condition for Fermi-level pinning at one of five experimentally identified energy levels (0.40 $\pm$ 0.04, 0.65 $\pm$ 0.02, 0.73 $\pm$ 0.02, 0.96 $\pm$ 0.04, and 1.18 $\pm$ 0.02 eV) at the metal/CdTe interface. To produce an efficient solar cell structure, the Fermi level should be pinned close to the valence band maximum (i.e., at 1.18 $\pm$ 0.02 eV below the conduction band minimum) and other unwanted defects should be eliminated by passivation.

The impact of various features of this model on the efficiency of the cell is considerable. The ability to obtain Fermi-level pinning near the top of the valence band enables the production of a barrier height of 1.18 $\pm$ 0.02 eV. This enables a high open circuit voltage to be achieved since V_{oc} is a function of the ϕ_b. Since this is an MS-type rectifying contact, the introduction of a thin insulating layer to form an MIS-type structure enables the further enhancement of the V_{oc} and lifetime of the device. One of the main reasons for the degradation of this device is the intermixing at CdTe/metal interface, but the insulating layer in this case acts as a reaction barrier to improve the lifetime of the device.

Since both window and absorber materials are n-type, doping with n-type dopants (according to the new model) instead of p-

type dopants (according to the p-n junction model) will improve the electrical conductivity of the device structure to enhance both the short circuit current density and the fill factor and, hence, enable the achievement of high efficiencies. In addition, this model would also explain the 'magic step' of the empirical $CdCl_2$ treatment necessary for achieving high efficiencies. According to this new model, halogens act as n-type dopants to both n-CdS and n-CdTe materials, reducing the series resistance in addition to observed grain growths to enhance device parameters. The improved understanding of material issues and physics behind this device will enable the PV community to further develop this device rapidly in the future.

The CdS/CdTe solar cell efficiency has stagnated at ~16% for more than two decades. With the improved understanding of the material issues and device physics, together with right experimental approaches, the efficiency of this device could exceed 20% in the near future.

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Chapter 5

Extension of the New Model to CIGS Thin-Film Solar Cells

5.1 Introduction

The material, copper indium gallium diselenide (CIGS) has attracted intense research within the PV community due to its high potential in thin-film solar cell development. This has been demonstrated by the report of 19.5% conversion efficiency in the year 2005 for lab-scale solar cell devices [1]. The efficiency has increased to 20.3% in 2010 [2], showing the gradual progress in the research and development front. However, further development of this device has been slow due to inadequate understanding in complex material issues, processing steps, and underlying solid-state physics principles of the device. This chapter summarises the current knowledge in these areas and proposes an improved device concept to describe the photovoltaic action of CIGS-based solar cells. Possible ways forward for further development of CIGS solar cells are also proposed.

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5.2 Summary of Accumulated Knowledge on CIGS-Based Materials

Worldwide research groups are working on CIGS-based materials and device structures to produce a low-cost and high-efficiency solar panel in order to convert solar energy directly into electricity [3–7]. In fact, a few institutes have already started the production of CIGS-based solar panels on an industrial scale. The following sections summarise the accumulated knowledge on this material to date before moving on to discuss the physics behind these solar cells.

5.2.1 *Different Growth Techniques*

Various techniques have been used to grow $CuInSe_2$ (CIS) and CIGS materials. The conventional semiconductor growth technique, or the melt-growth method, has been used to grow bulk materials [8–9] in order to study their structural, optical and electronic properties.

Thin films of CIGS have also been grown by the flash evaporation [10], vacuum evaporation [11, 12], electrodeposition [13–17], and spray pyrolysis [18] techniques. The most commonly used method is the deposition of Cu, In, and Ga layers and then the incorporation of Se through the selenisation process. Some groups also incorporate S into the layer in order to engineer the bandgap of this material and hence increase the performance efficiency of CIGS solar cells [19].

5.2.2 *Structural, Optical, and Electronic Properties*

Most layers produced for large-area device production show a chalcopyrite structure with polycrystalline nature. The grain sizes vary in the sub-micron and micron regions, depending on the growth conditions used. This material has a direct bandgap, and its value can vary between $\sim$1.00 eV (the bandgap of CIS) and $\sim$1.68 eV (the bandgap of $CuGaSe_2$), depending on the composition of the layer. Since this alloy contains four or five elements, the control of composition and, hence, its bandgap is a challenging task. However, many research groups have achieved excellent devices, in excess of 15% efficiency, with materials having bandgap values in the range

~1.20–1.45 eV. Most research groups report the CIGS layers used in the solar cell devices as p-type materials.

5.2.3 *Ordered Defect Compound Layer*

The natural formation of a Cu-deficient (In-rich) surface layer on CIGS material has been observed by many researchers [20–22], and reports agree in general, with a few exceptions. The reported thickness of this ordered defect compound (ODC) layer is ~15 nm, and this surface layer is n-type in electrical conduction with a bandgap of ~1.30 eV. Since this has been observed in all CIGS materials grown using different techniques, this must be due to a natural occurrence taking place near the surface. This surface layer can play a considerable role in device performance and, therefore, device designs must consider this well-known natural phenomenon and use it to the device's advantage.

Both In (melting point = 156.6°C) and Ga (melting point = 29.8°C) metals are solids at room temperature, but when brought together, they readily form an In-Ga eutectic, which is a liquid at room temperature. Perhaps for this reason, the CIGS alloy can be formed easily by the selenisation of a soft alloy within a short period of time. For the same reason, and other yet-unknown thermodynamical properties, Cu atoms diffuse into the crystal, away from the free surface, forming this experimentally observed ODC layer.

5.2.4 *Latest Developments in Materials Growth*

Publications between 2004 and 2007 on the electrodeposition of CIS [23] and CIGS [24, 25] reported a controlled way of growing p^+, p, i, n, and n^+ material layers for the first time. This electrical conduction type variation can be achieved by controlling the chemical composition of the material layers. These results are summarised in section 3.4.3 in chapter 3. In CIS material, Cu (Group-I element) richness provides p-type electrical conduction and In (Group-III element) richness provides n-type electrical conduction. In the case of CIGS material, although Ga is a group-III element very similar to In, addition of Ga makes the material more p-type. This is purely an experimental observation from the recent

work on electrodeposition of CIGS material [24, 25]. For example, GaSe is always a p-type semiconductor [26]; therefore, Ga must be producing acceptor-like native defects in the material instead of acting as a simple substitutional n-type dopant. However, the amount of Ga added to the material is helpful in reducing n-doping due to In addition and increasing the bandgap of the compound alloy. By controlling the atomic concentration of In and Ga, suitable doping levels for devices and the energy bandgap can be achieved.

5.3 Summary of Accumulated Knowledge on CIGS-Based Solar Cells

Most research groups follow the conventional substrate-type device structure to develop CIGS-based solar cells. This section summarises the device structure, current understanding of the physics behind this device, reported device performance, and some notable features leading to a new understanding of the solid-state principles behind these devices.

5.3.1 *Conventional Device Structure*

The CIGS solar cell device, currently under intense research has a glass/Mo/CIGS/n-CdS/i-ZnO/n-ZnO:Al/metal-grid structure. A schematic diagram of the complete structure for this device is shown in Fig. 5.1. The device is gradually built up starting from the back metal contact of Mo, sputtered on to the glass substrate. The growth process of CIGS varies, and the most common techniques used are co-evaporation of elements or sputtering to deposit individual Cu, In, and Ga layers and then selenise at temperatures above 550°C using H_2Se gas [19]. Some groups introduce S also on to the surface by the sulphidation process at 600°C using H_2S gas [19]. After the completion of the growth of the CIGS layer, a thin layer of n-CdS (~80 nm) is incorporated usually using the chemical bath deposition (CBD) technique. Intrinsic ZnO (~70 nm) and an n-type Al-doped ZnO (~100 nm) layers are then deposited using the sputtering technique. A grid type Al/Ni front metal contact is finally deposited by either the vacuum evaporation or sputtering technique.

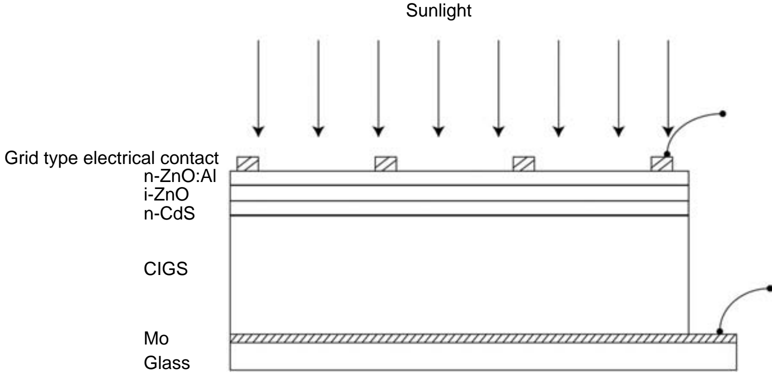

Figure 5.1 A schematic diagram of a thin-film CIGS solar cell showing the main components of the device structure (not to scale).

5.3.2 *Frequently Used Energy Band Diagram*

In order to describe the PV action, a rectifying interface available within the device structure should be identified. The frequently used energy band diagram for this purpose is shown in Fig. 5.2, and the research directions are usually guided according to this device concept. The analysis of experimentally observed results, scientific thinking, and the future development programmes are heavily dependent on this device concept. In the scientific research process, it is essential and a good practice to examine the existing wisdom from time to time to check their accuracy. Otherwise, errors could propagate through the scientific literature, hindering positive progress. Careful and close observation of this energy band diagram raises two main concerns.

(i) This energy band diagram has been constructed using Anderson's electron affinity rule and the electron affinity values of semiconducting materials used. By taking the vacuum level as the reference and the electron affinity of ZnO, the conduction band edges of both i-ZnO and n-ZnO:Al have been drawn accurately. However, this contradicts the most important solid-state physics principle of the position of the Fermi level of i-ZnO.

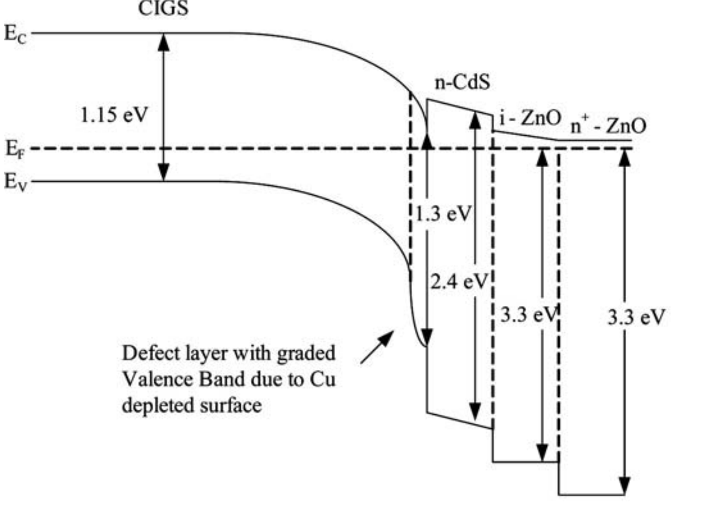

Figure 5.2 The energy band diagram used to explain the PV activity of thin-film CIGS solar cells.

The Fermi level should be in the middle of the energy gap for i-ZnO, and this condition is not satisfied here, in this diagram.

(ii) This diagram also does not represent the actual scale of space on the horizontal axis. In these devices, the CIGS layer is about 3,000 nm and the combined (n-CdS + i-ZnO + n-ZnO:Al) layer is about 300 nm in thickness. Therefore, the CIGS to the combined layer should have the scale of 10:1 in this diagram. This real space relationship is not shown in this diagram; therefore, it appears to be a genuine p-n-type hetero-junction between p-CIGS and n-CdS, providing an incorrect impression. When drawn to scale, the combined layer becomes extremely thin when compared to the CIGS layer, indicating this as the insulating component of an MIS-type electrical contact.

5.4 Current Views of the Physics Behind CIGS Solar Cells

It is of paramount importance to understand the solid-state physics principles underpinning these devices in order to systematically

develop these solar cells. A literature search on this subject clearly shows different views expressed from various research groups active in this field. The following sections present three different models proposed to date to describe the PV action of this device.

5.4.1 *p-CIGS/n-CdS Hetero-Junction*

The most widely assumed concept is the hetero-junction formed between p-type CIGS material and the n-type CdS layer. Most of the research and analysis carried out to date are based on this hetero-junction concept. These explanations are relevant if the energy band diagram shown in Fig. 5.2 is accurate.

5.4.2 *p-CIGS/n-CIGS Homo-Junction*

In the above device structure, the thickness of n-CdS layer varies in a wide range, from 10 nm [27] to 85 nm [28]. In all cases, the device shows PV activity, and the best performance is usually given by devices with extremely thin layers (10–85 nm) of CdS. It is well established that the surface and interface chemistry of electronic devices observed using soft-XPS work show that these interfaces are highly intermixed due to chemical reactions and in- and out-diffusion of semiconductor elements across the boundary. Therefore, about 80 nm thick layer of CdS is not sufficient to form a CdS crystal lattice after consumption within interfaces and, hence, to form a well-defined energy bandgap. For these reasons, some groups [29] have suggested that the n-CdS layer can only be a surface passivation layer and that the rectifying interface may be a buried homo-junction within the thick CIGS layer (of about 3 μm). However, this proposed idea has also not been proved by experimental or theoretical means. This property cannot be seen from Fig. 5.2 since a much thicker CIGS layer is not shown in this diagram.

5.4.3 *p-CIGS/n-ODC Hetero-Junction*

As discussed in section 5.2.3, the formation of a thin layer of Cu-deficient or In-rich surface layer is due to a natural phenomenon related to Cu diffusion away from the free CIGS surface. This ordered

defect compound layer also has an n-type electrical conduction and a bandgap of ~1.30 eV. Therefore, several research groups have proposed a possibility of the formation of a hetero-junction between the p-CIGS and n-ODC layers. This concept has also not been experimentally or otherwise confirmed to date, but the idea is floating around in the research community. But the observations of Fig. 5.2 show that the natural ordered defect compound (ODC) layer with n-type electrical property sets well within this energy band diagram between p-CIGS and n-CdS layers. Such layers with ordered defects at interfaces in electronic devices could produce defect levels with high concentrations and could firmly pin the Fermi level in these structures. This will be discussed in later sections of this chapter.

5.5 Reported Device Performance

The device structure described above remains the same for different research groups, but material production processes and layer thicknesses used have slight differences. As a result, the device performance shows a wide variation, making it difficult to recognise any specific patterns. In order to identify systematic patterns, it is important to consider only results reported for best performing devices. Table 5.1 summarises the results reported for solar cells showing efficiencies greater than ~12%.

Table 5.1 A summary of open circuit voltage values reported by different research groups for devices showing efficiencies in excess of ~12%

Reference	V_{oc} Values Reported (V)	Identified Group
M. A. Contreras *et al.* [1]	(0.42–0.55), ~0.65, ~0.75, (0.80–0.90)	A B C D
S. Ishizuka *et al.* [30]	~ 0.70	C
D. Rudmann *et al.* [31]	(0.60–0.68)	B
D. Ohashi *et al.* [32]	(0.48–0.52), ~0.62	A B
T. Nakada *et al.* [33]	~ 0.53	A
Y. Nagoya *et al.* [34]	~ 0.55	A
O. Lundberg *et al.* [35]	~ 0.65	B
T. Nakada *et al.* [36]	~ 0.60	B

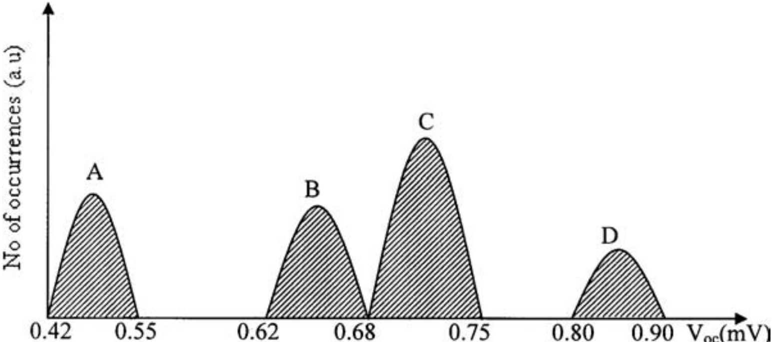

Figure 5.3 Four main experimentally observed groups of open circuit voltages appearing in CIGS-based solar cells.

The observation of the results summarised in Table 5.1 shows that the V_{oc} values measured tend to appear in several groups. These experimentally observed groups of V_{oc} values are graphically shown in Fig. 5.3 and labelled as A, B, C, and D. The most striking observation is that there are four different reported V_{oc} values in reference [1]. The open circuit voltage is a function of the potential barrier height (ϕ_{b}) of the device, as given by Eq. 1.16.

$$V_{\text{oc}} = n\left\{\phi_{\text{b}} + \frac{kT}{e}\ln\left(\frac{J_{\text{sc}}}{AT^2}\right)\right\} \tag{5.1}$$

The different groups of V_{oc} are observed due to discrete variation in barrier heights, which depends on materials and processing conditions. This identification is a key to better understanding of the physics behind the device structure. It must be stressed that for the identification of these discrete V_{oc} values, only the results of high-efficiency CIGS solar cells should be considered. In the case of low-efficiency CIGS solar cells, these groups merge together, making it even more difficult to identify any pattern.

In all of the above cases, whether it is a homo-junction or a hetero-junction, each situation should produce only one group of V_{oc} value for high-quality devices. How we experimentally observe several groups of V_{oc} values is an unanswerable question based on conventional homo- and hetero-junction devices. This will be further discussed in section 5.7 using an improved concept for this device.

This is in fact the extension of the new model proposed recently by Dharmadasa *et al.* [37, 38, 39] for CdS/CdTe thin-film solar cells.

5.6 Recent Work on Metal/p-CIGS Interfaces

The metal/semiconductor (MS) interface plays an important role in electronic transport across device structures, as described in chapter 1. However, work on metal/CIGS interfaces is very scarce in the literature. One reason for this may have been the non-availability of high electronic quality CIGS reference materials for this work. One of the papers published in 2005 [39], however, is noteworthy in this work on p-type CIGS materials grown by Showa Shell in Japan [40]. Since this material produced over 13% conversion efficiency for large-area (3,600 cm^2) solar panels in the year 2003, the author's group selected this high-performance p-CIGS material for electrical contact studies. This work investigated metal/p-CIGS interfaces in detail using Ag ($\phi_m = 4.26$ eV), Cu ($\phi_m = 4.70$ eV), and Au ($\phi_m = 5.10$ eV) covering a wide range of metal work functions (φ_m). The final results are summarised in Table 5.2 and in Fig. 5.4, clearly showing four main discrete Fermi-level pinning positions. This situation is identical to the one observed for n-CdTe/metal interfaces [37–39, 41], as described in chapter 4.

A comprehensive literature search shows that these Fermi-level pinning positions overlap with the major defect levels independently observed for CIGS using current-voltage (I-V), capacitance-voltage (C-V), photoluminescence (PL), deep-level transient spectroscopy (DLTS), photo acoustic spectroscopy (PAS), and

Table 5.2 The ideality factor (n) and the ϕ_b (eV) measured for 2 mm diameter metal contacts fabricated on chemically etched $Cu(InGa)(SeS)_2$ layers

Ag		Cu/Au		Au	
n	ϕ_b (eV)	n	ϕ_b (eV)	n	ϕ_b (eV)
—	—	1.40–2.20	0.75–0.79	—	—
1.57–3.29	0.82–0.87	1.74–2.90	0.82–0.85	1.60–2.60	0.83
1.24–1.80	0.93–0.95	—	—	—	—
1.24–1.53	1.01–1.04	—	—	—	—

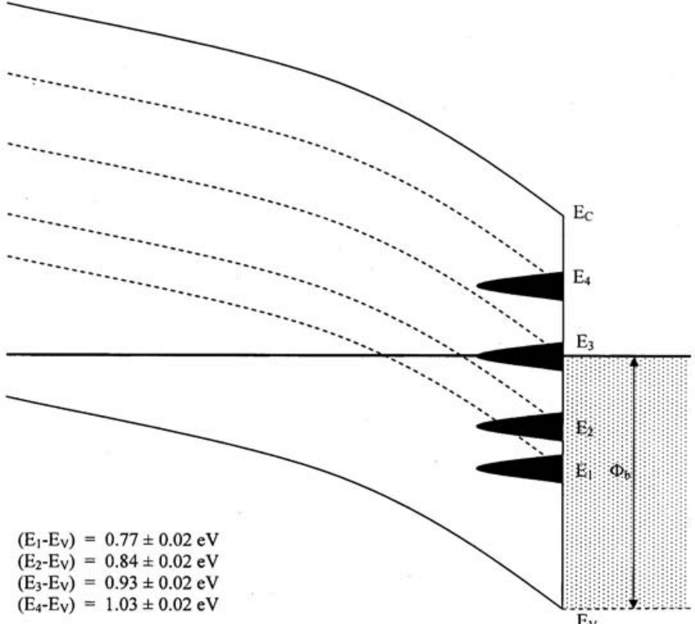

Figure 5.4 Experimentally observed Fermi-level pinning positions for metal/p-CIGS interfaces [39].

cathodoluminescence (CL) techniques. These results are summarised in Table 5.3 for comparison, and it is remarkable to observe the closeness of these defect levels in CIGS material. It is also apparent that the PAS technique is capable of identifying closely spaced defect levels in semiconductors.

Table 5.3 A summary of the defect levels independently observed for CIGS materials from different research groups, using six different techniques

Energy Level (eV)	**Schottky Barriers [39]**		**PL [42]**	**DLTS [43]**	**PAS [44]**	**CL [45]**
	(I-V)	(C-V)				
(E_1-E_V)	0.77 ± 0.02	—	—	—	0.75–0.78	—
(E_2-E_V)	0.84 ± 0.02	—	0.85	0.87	0.82–0.86	—
(E_3-E_V)	0.93 ± 0.02	—	0.94	—	0.90	0.97
(E_4-E_V)	1.03 ± 0.02	1.03	(1.00–1.17)	1.03	1.01	1.08

5.7 Deeper Understanding of Mo/CIGS/CdS/i-ZnO/n-ZnO:Al/Metal-Grid Solar Cells

The main clues for the new model are provided by the results summarised in Table 5.3, Fig. 5.4 [39], and the discrete V_{oc} values observed for the same device structure (Fig. 5.3). A comprehensive CIGS material characterisation [46], together with I-V and C-V experiments carried out on metal/p-CIGS interfaces [39], confirm strong Fermi-level pinning behaviour depending on surface treatment differences and the position of the 2 mm diameter metal contact fabricated on the CIGS layers (due to non-uniformity of the material). If this is the case, the production of discrete V_{oc} values is expected since this parameter is a function of ϕ_b. There is an excellent agreement of ϕ_b measurements, together with independent defect-level measurements from different groups, using different techniques (Fig. 5.4 and Table 5.3).

The formation of a PV-active device structure depends on the fine details of the materials growth and device processing. Careful observation of the experimental results reported in the literature shows the formation of two types of PV solar cells based on CIGS material. These two types of devices are described below.

5.7.1 *Type-I CIGS-Based Solar Cell*

The Showa-Shell CIGS materials are produced by the deposition of Cu, In, and Ga layers on glass/Mo substrates, and the subsequent selenisation at 550°C, followed by sulphidation at 600°C. The material produced is p-type in electrical conduction, and the full characterisation results of this material were published in the year 2004 [46]. Using the p-type conduction of the CIGS material and Fermi-level pinning at discrete levels, the band diagram for this type of device is presented in Fig. 5.5. The (a) n-type ODC layer, (b) n-type CdS layer, (c) i-type ZnO layer, (d) n-type Al-doped ZnO layer, and the front metal contact are shown in the energy band diagram. The increased bandgap of CIGS material towards the front of the solar cell due to the introduction of S is also shown in the band diagram. The formulation of this band diagram is based on the Fermi level pinned at one of the defect levels (E_4), and the reference level has been taken

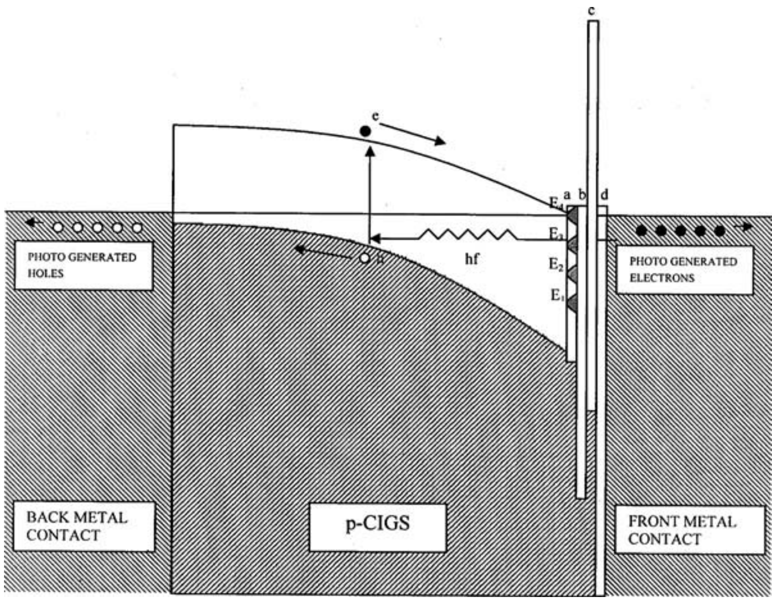

Figure 5.5 An energy band diagram for the type-I solar cell for back metal contact/p-CIGS/ODC layer(a)/n-CdS(b)/i-ZnO(c)/n-ZnO:Al(d)/front metal contact structure. The conditions shown are for short circuit situation under illumination.

as the Fermi level. The bandgap energy values of the different material layers are approximately according to scale, and the thickness of CIGS (~3,000 nm) and the four layers (~300 nm) between CIGS and the front metal contact shows a ~10:1 ratio in thickness. Therefore, the device is basically a large Schottky diode on p-CIGS with an MIS-type electrical contact containing a thick compound I-layer.

In theoretical modelling with ideal semiconductors, it is normal practice to use the vacuum level as the reference energy level according to the Anderson's electron affinity rule. Once the vacuum level has been taken as the reference, the electron affinity (χ_S) values of semiconductors decide the location of the conduction band minima, resulting in band bending and, therefore, the energy band diagram. Although this is valid for ideal situations, it is more accurate to use the Fermi level as the reference level, especially when the Fermi level is pinned in practical devices. Therefore, in this book, all the band

diagrams formulated are with respect to the Fermi level, which is pinned at one of the experimentally observed native defect levels.

Depending on the fine details of the growth of CIGS material, processing steps, and metallisation, the Fermi level will be pinned at one of the four experimentally observed defect levels. The ϕ_b is, therefore, defined by the Fermi-level pinning position. When the Fermi level is pinned at E_4 level, the best solar cell is formed with p-CIGS. If the Fermi-level pinning is at the E_1 level, the device will have the least band bending and, hence, poor performance of the device. Depending on the pinning position, discrete V_{oc} values will be observed.

In Fig. 5.5, the bandgap has been increased towards the front of the solar cell due to the addition of S. Also, the ODC layer with a ~1.30 eV bandgap is naturally helping for the efficient creation, separation, and collection of charge carriers. Since the naturally occurring ODC layer is In-rich and n-type in electrical conduction, the Fermi level is automatically pulled closer to the conduction band minimum. The experimentally observed E_4 defect level may be due to these Cu deficiencies in the vicinity of the p-CIGS surface. It is interesting to compare the experimentally observed potential barrier heights for good solar cells based on CIGS material. These barrier heights are usually in the region of 1.14 eV. The Fermi-level pinning at the E_4 level created by the ODC layer produces ~1.03 eV Schottky barrier (see Fig. 5.4) and the rest is provided by the effect of the MIS contact used. The naturally occurring ODC layer has been very helpful in producing high efficiency solar cells fabricated on CIGS.

The three layers (n-CdS, i-ZnO, and n-ZnO:Al) are an interesting combination. They form a compound I-layer in order to form an MIS-type solar cell structure. This increases the effective ϕ_b and, hence, an improved V_{oc} value when compared to a device with MS contact. However, it should be noted that the thickness of this compound I-layer (~300 nm) is much larger than that of conventional MIS structures. This is still acceptable, since both n-CdS and n-ZnO:Al are two semiconducting layers with comparatively large electrical conduction. The insulating layer, i-ZnO, sandwiched between the two semiconductors will have a thinner layer due to interface interactions on both sides.

The i-ZnO layer has a three-fold function in this case. Since this is an insulating layer, this material fills all pinholes in the structure and reduces shorting of devices, increasing the production yield and initial efficiency of the device. The second function is to contribute to the compound insulating layer to form MIS-type electrical contact, improving V_{oc}. The third function is the most interesting one. It should be noted that at the interfaces of these layers, intermixing and in- and out-diffusion take place during growth, processing, and ageing. Therefore, their effective thicknesses are much less than the initially deposited values. The layer (c) is, therefore, thin enough for optically generated and accelerated electrons to tunnel through but acts as a barrier layer for the back diffusion of photo-generated and separated electrons in the front metal contact. Therefore, this layer can be labelled as an electron back diffusion barrier (ebdb) layer. The presence of this layer reduces the back diffusion of electrons over the potential barrier to recombine with photo-generated and separated holes present in the back metal contact. This prevention will improve the open circuit voltage of the device and, hence, J_{sc} and other device parameters. A thicker ebdb layer will hamper electron transport to the front contact and add to series resistance, causing the deterioration of device parameters.

In a similar way to an ebdb layer, both (b) n-CdS and (d) n-ZnO:Al layers are acting as hole back diffusion barrier (hbdb) layers. Their presence in the device, therefore, minimises the hole transfer to the front contact and the recombination of photo-generated and separated charge carriers by thermionic emission over the potential barrier.

5.7.2 *Type-II CIGS-Based Solar Cell*

There is another type of device developed at NREL in the United States and several other laboratories. The band diagram for this second type is shown in Fig. 5.6. This type-II device has a Cu-rich electrodeposited CIGS (~2.2 μm) on the Mo back contact [1]. The work reported by the author's group in 2004 and 2007 proves without ambiguity that this material with Cu richness is p-type in electrical conduction [24, 47, 48]. Note that there are at least two papers reporting Cu-rich material as n-type [49, 50], but more recent

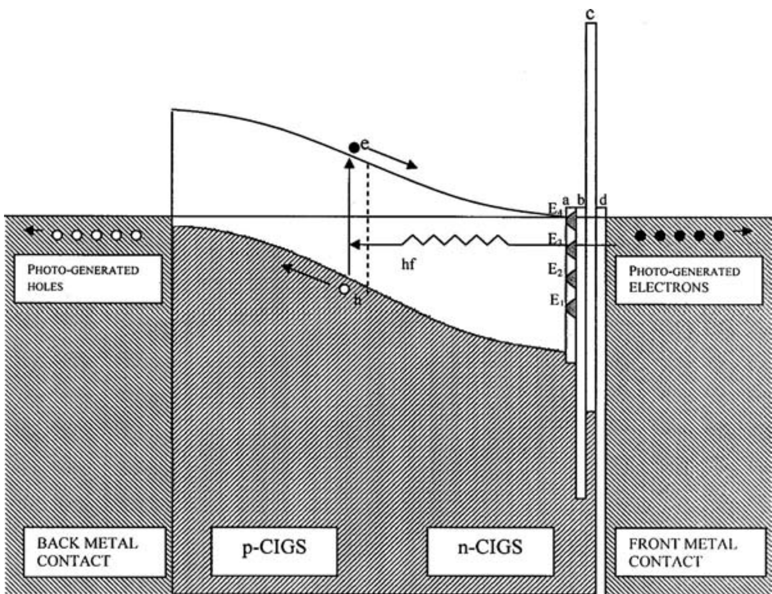

Figure 5.6 An energy band diagram for type-II solar cells with back metal contact/p-CIGS-n-CIGS/ODC layer(a)/n-CdS(b)/i-ZnO(c)/n-ZnO:Al (d)/ front metal contact. The device is a combination of a p-n junction and an MIS structure at the front contact.

and comprehensive work clearly confirms that it is not the case [23, 24, 47, 48]. According to solid-state physics principles, Cu richness should produce p-type CIGS and this has now been thoroughly proven by experimental work. The second stage of the NREL process is to deposit In and Ga layers (~1.5 μm) by the physical vapour deposition (PVD) process and selenise these metallic layers. The electrical conductivity type depends on the ratio of In and Ga elements. If more Cu and Ga are present, the second half of the layer will become p-type and, consequently, the whole CIGS layer will be p-type, forming the type-I device, as shown in Fig. 5.5. If In content is high, the second half of the CIGS layer becomes n-type and forms a p-n homo-junction, as shown in Fig. 5.6.

In addition, the Fermi-level pinning takes place at the front metal contact very similar to the type-I device structure. A type-II device has an added advantage over the type-I solar cell structure. This

is a combination of p-n homo-junction and an MIS-type electrical contact, improving the charge carrier creation, separation, and collection into the external circuit.

In both type-I and type-II cases, Fermi-level pinning at different levels produces discrete V_{oc} values with varying performance. The most desirable pinning position is at E_4 in order to produce a solar cell with the highest V_{oc}. Since there are four possibilities for Fermi-level pinning, four potential barriers and, hence, four groups of V_{oc} values can be expected. This has in fact been experimentally observed, and the results are shown in Fig. 5.7. These groups can

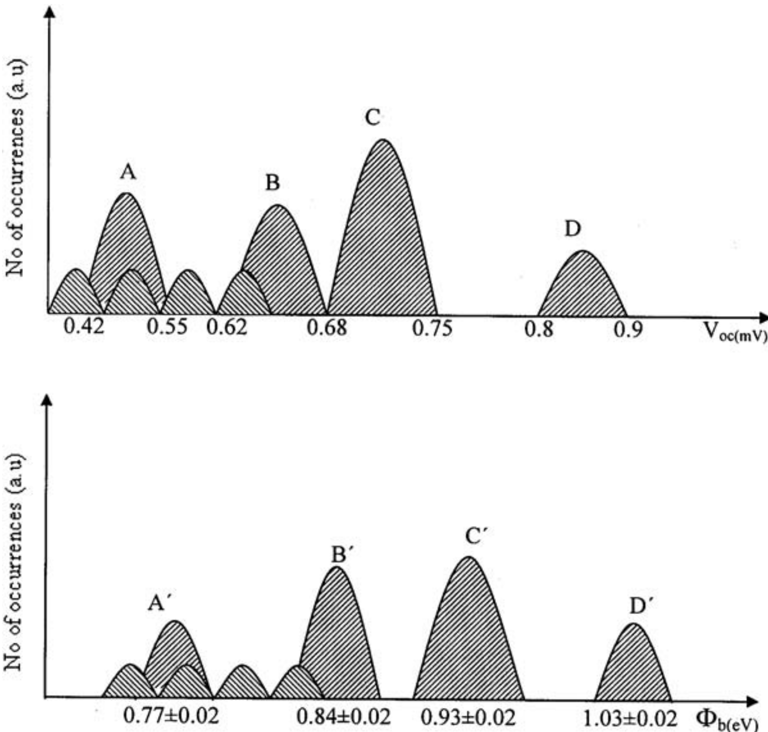

Figure 5.7 Four different experimentally observed main groups (A, B, C, D) of open circuit voltages and corresponding groups of potential barrier heights possible due to Fermi-level pinning at discrete defect levels in CIGS solar cells. Additional defect levels in the vicinity of groups A' and B', observed by more sensitive PAS technique, are also shown.

only be identified separately for good devices with high efficiencies. If the device performance is poor due to various other reasons, V_{oc} values will merge together, making it hard to identify different groups. It is also apparent that there are four closely spaced defect levels, as observed by the PAS technique, available in the vicinity of groups A' and B'. This may produce a continuous range of V_{oc} values between groups A and B instead of producing discrete V_{oc} values.

The Fermi-level pinning effect tends to produce discrete barrier heights and, hence, different groups of V_{oc} values. However, the presence of MIS structure broadens each group and makes it hard to identify discrete nature. Only careful observations of high-efficiency solar cells will help in identifying this pattern in CIGS solar cells.

5.8 Discussion on Further Improvements of CIGS Solar Cells

Based on this concept, it is now possible to propose ways of improving the device efficiency. There are several different approaches, and they are discussed under the following headings.

5.8.1 *Optimisation of Growth, Doping, and Bandgap Engineering*

In both situations, the first part of the absorber material (CIGS) should be grown with Cu richness. It is well known that Cu-rich CIGS have large grains and high electrical conduction. The large grains provide a better substrate for subsequent material layers to grow well, and high electrical conduction helps in the formation of a low-resistance ohmic contact to Mo back contact. Gradual increase of the bandgap can be obtained by adding In, Ga and S. These graded bandgap structures are shown in both Figs. 5.5 and 5.6 for effective charge carrier creation, separation, and collection. The addition of In makes the CIGS material n-type, and the inclusion of Ga makes the CIGS layers p-type. Therefore, by varying the In and Ga content, the doping concentration can be optimised in principle, although challenging. In order to produce a depletion region of $\sim$2–3 μm, to cover the full depth of the device, the doping concentration needs to

be in the low 10^{15} cm^{-3} values [51]. By achieving these optimum doping concentrations and bandgap engineering, a healthy device structure can be produced for effective PV solar energy conversion utilising minimum thickness of the material layers. Because of the excellent optical absorption property of CIGS, only a ~3 μm thick absorber layer is required for this solar cell.

5.8.2 *Defect Level Identification and Engineering*

As shown in Fig. 5.5 and 5.6, the most desirable position for Fermi-level pinning is at the E_4 level. This provides the optimum band bending required for charge carrier collection. Fortunately, many device structures with CIGS show a ϕ_b of ~1.10 eV, indicating the most common pinning position is at the E_4 level.

The identification of other defect levels has paramount importance. Once identified, ways of passivation or removal of these levels should be explored. The presence of the E_1, E_2, and E_3 levels deteriorates the device parameters either by pinning at these undesirable levels, causing low V_{oc}, or through contributions to R&G process, causing low J_{sc} values for high V_{oc} devices obtained with Fermi-level pinning at the E_4 level.

From the accumulated knowledge to date, it seems that the E_4 level, close to the conduction band is related to the n-type ODC layer. Since this layer is Cu-deficient, and n-type in electrical conduction, the E_4 defect level must be associated with Cu deficiencies (Cu vacancies) or In richness. Fortunately, it seems that this natural phenomenon is helping to produce a good device by pinning the Fermi level at the most desirable native defect level of E_4 close to the conduction band minimum.

5.8.3 *Growth of CIGS with Controlled Orientation*

All CIGS layers used in thin-film solar cells are polycrystalline, and XRD patterns show three major reflections, at (112), (220/204), and (116/312). It has also been shown that controlling the growth process leads to the production of materials with (112)- or (220/204)-preferred orientations. The work reported in 2004 by Ott *et al.* [45] explains different defect structures using CL

work for (112)- and (220/204)-preferred-oriented CIGS layers. This work shows the dominance of the defect level at 0.97 eV (E_3) for (112)-oriented films and 1.08 eV (E_4) for (220/204)-oriented films. This clearly indicates that the Fermi-level pinning at E_4 will take place for (220/204)-preferred-oriented layers, producing better performance than (112)-oriented CIGS layers. This observation needs further exploration and systematic research for efficiency to be maximised by the selection of more advantageous crystal orientations.

5.8.4 *Replacement of Mo Using TCO for Tandem and Double-Faced Solar Cells*

In the conventional device, the Mo back contact is an opaque metal contact with a thickness of $\sim$1 μm. However, the same device structure can be developed on glass/transparent conduction oxide (TCO) substrates instead. In this case, the solar cell can be used for both tandem [52] and bi-facial solar cells. Therefore, this double-sided illuminated solar cell will produce more electric power from a given panel at least for some applications. Bi-facial solar cells will be more attractive for applications with vertically fixed solar panels in unshaded areas for power generation. This type of CIGS solar cells will also help in development of high voltage tandem solar cells for use in solar hydrogen production by the electrolysis of water.

5.8.5 *Further Improvements of the Device Structure*

In both device structures, the i-ZnO layer plays several important roles. However, this layer is hampering current collection due to its present position at (c). Both these device structures can be improved by adding an ebdb layer at the back contact and an hbdb layer at the front metal contact. In addition, it is useful at the current position in order to act as a pinhole plugging material. This improved device structure for type-II device is shown in Fig. 5.8 and will produce enhanced device parameters.

The back metal contact (Mo) used in the traditional CIGS solar cell in fact, already has this advantage built into the device. The research published in the literature shows the natural formation of

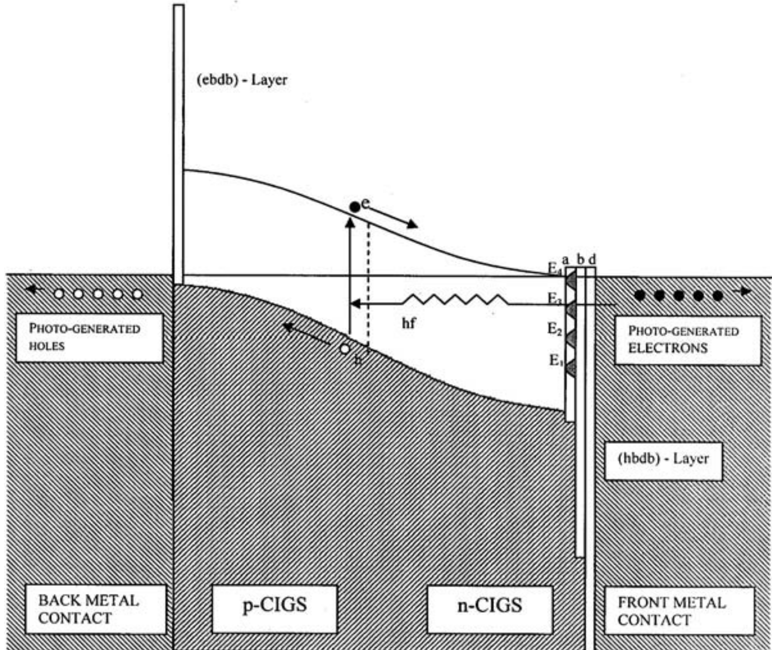

Figure 5.8 An improved energy band diagram for enhanced charge carrier separation and collection, incorporating ebdb and hbdb layers.

$MoSe_2$ at the Mo/CIGS interface. This compound is a p-type material with a wide bandgap ($E_g = 1.40$ eV) and semiconducting properties [53–56]. These two properties, in fact, ideally produce the required ebdb layer at the Mo/CIGS interface, as shown in Fig. 5.8. This is another good reason for the conventional device structure to perform well to date.

5.9 Conclusions

This chapter has summarised and presented the current knowledge on CIGS-based material issues, device processing stages, and device physics principles for describing CIGS-based thin-film solar cells currently under the research and development stage. This review, therefore, leads to the following main conclusions.

(a) CIGS material can be grown by several different techniques, and its bandgap value can be engineered between ~1.00 eV and ~2.20 eV. Since five different elements are involved in this alloy, the control of composition and, hence, uniformity and reproducibility remain a challenging task.
(b) In a CIGS material sample, Cu atoms are driven away from the free surface towards the bulk of the material due to yet unknown natural phenomenon. As a result an In-rich, n-type and, wider bandgap material layer is formed at the surface. This is known as the ODC layer among the PV community and naturally helps in the formation of the device by pinning the Fermi level at E_4, close to the conduction band minimum.
(c) The work reported in 2004 and 2007 on the electrodeposition of thin CIS and CIGS layers has shown that the predetermined p^+, p, i, n, or n^+ materials can be grown by controlling its chemical composition. As solid-state physics principle guidelines, p-type materials are produced when the material is rich in Cu (In-deficient), and n-type materials are produced when the material is rich in In (Cu-deficient).
(d) The electrical contact work on CIGS material is almost non-existent, but the work reported in 2005 on metal/p-CIGS shed light on understanding physics behind this device. Strong Fermi-level pinning is evident; therefore, the new model proposed for the CdS/CdTe solar cell in the year 2002 is also applicable to CIGS-based solar cells.
(e) Three different proposed models (based on n-CdS/p-CIGS hetero-junction, n-ODC layer/p-CIGS hetero-junction, and n-CIGS/p-CIGS homo-junction) are currently in use for this device, indicating the complexity of the device structure. In fact, all these three proposed ideas are embedded in the energy band diagram shown in Fig. 5.6. In addition to the combination of these three ideas, Fermi-level pinning at discrete positions and an MIS-type structure at the front electrical contact have made it even more complex to visualise and understand.
(f) There are two types of devices under development today. The type-I is based on p-CIGS, and this is mainly due to an MIS-type solar cell with four Fermi-level pinning possibilities. The type-II is more efficient in charge carrier creation, separation, and

collection and based on the combination of a p-n homo-junction and an MIS-type front contact. In both cases, the I-layer is a compound layer made out of n-ODC, n-CdS, i-ZnO, and n-ZnO:Al layers. The n-ODC layer is naturally supporting both devices for Fermi-level pinning at the E_4 level and creating required band bending.

(g) Because of the four main Fermi-level pinning positions, the ϕ_b can vary from batch to batch or device to device depending on the material quality and processing steps. Therefore, the open circuit voltages of good devices can show discrete values as observed and reported in the literature. For poor devices, V_{oc} values will be merged together, making it impossible to identify this pattern.

(h) With this improved understanding, the device can be further developed by adding ebdb and hbdb layers into the device structure, optimising the doping concentration and engineering the bandgap of material layers used. In addition, the identification of defect levels responsible for Fermi-level pinning and removal or passivation of undesirable defect levels will lead to high performance CIGS solar cells.

5.10 Summary

This review chapter summarises the knowledge accumulated in the literature on CIGS material and solar cells based on CIGS. After reviewing the present use of solid-state physics principles to describe thin-film solar cells based on CIGS, an improved concept is proposed with the aid of advances in the field on electrical contacts to CIGS material. It has been shown that the Fermi-level pinning takes place at one of the few experimentally observed defect levels. The main levels observed are at 0.77, 0.84, 0.93, and 1.03 eV with ± 0.02 eV error and are situated above the top of the valence band. As a result, discrete values of open circuit voltages are observed and the situation is very similar to that of CdS/CdTe solar cells described in chapter 4. Based on this new concept, different ways for further development of CIGS solar cells are proposed and this device has high potential to achieve much higher conversion efficiencies.

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Chapter 6

Effective Harvesting of Photons

6.1 Introduction

The market penetration of photovoltaic (PV) solar technology is hindered by its high cost, and various new methods have been introduced to overcome this barrier. High efficiency multi-layer tandem solar cells, new low-cost materials and device structures, and the mass production of PV modules are some of them. In the case of tandem solar cells, the present trend is to move from one-junction devices to double-junction, triple-junction, and multi-junction structures in order to enhance the absorption of photons from the solar spectrum. The current method is to use tunnel junctions to combine several cells made out of materials with different bandgaps. This chapter presents disadvantages of the current practice of using a tunnel junction approach and introduces an alternative method of effective harvesting of photons to achieve higher conversion efficiencies.

6.2 Tandem Solar Cells

The main aim of the tandem solar cell is to absorb a major part of the solar spectrum and, hence, increase the efficiency of the device by

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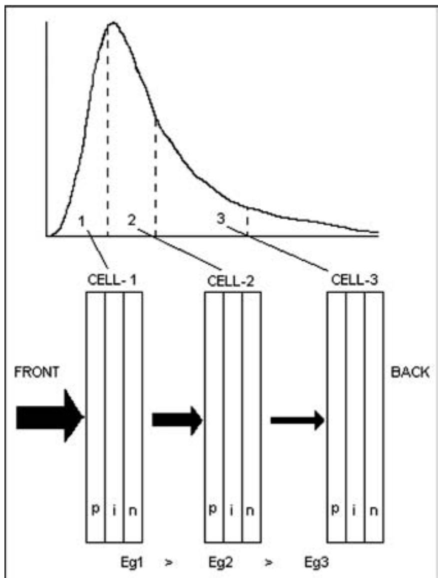

Figure 6.1 The approximate shape of the solar spectrum and arrangement of three different p-i-n diodes to absorb photons in three regions. The bandgap within one cell is constant, but the materials in cell-1 have larger bandgaps than those in cell-3.

increasing the short circuit current density. The approach is to fabricate p-n, p-i-n, or any other diode structure with different bandgap semiconductors and connect them to enhance the PV conversion. As shown in Fig. 6.1, cell-1, at the front, is fabricated with a wide bandgap material to convert high-energy photons from the blue-end, while cell-3, at the back, is fabricated with a narrow bandgap material to convert low-energy photons from the infrared (IR) end.

In this tandem solar cell approach, the next step is to connect the cells together to form one tandem solar cell device. There are two possible ways of achieving such a tandem solar cell — either by connecting them in series or in parallel configuration.

6.2.1 *Connection in Series*

This type of connection is widely used today by connecting adjacent devices in series using a tunnel junction. A schematic diagram of

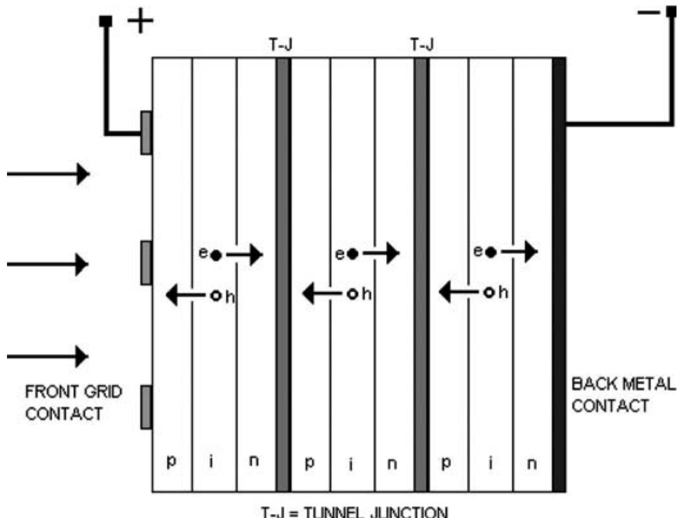

Figure 6.2 A schematic diagram of a tandem solar cell fabricated by connecting three p-i-n diodes in series through two tunnel junctions. See also Colour Insert.

such a tandem solar cell is shown in Fig. 6.2, and the corresponding energy band diagram is shown in Fig. 6.3. In this series connection, the n-type material of one device is connected to the p-type material of the adjacent device (Fig. 6.2). In other words, the conduction band of one device is placed very close to the valence band of the adjacent device (Fig. 6.3). The idea is to convert photons with different energy ranges in the three different devices and collect the charge carriers efficiently to generate high power in the external circuit. Since the solar cells are connected in series, the output voltages will add up and the current through the system will be constant. Therefore, for best results, the current produced by the three individual cells should be equal and hence current matching is important in this case.

6.2.2 *Connection in Parallel*

The other approach to fabricating a tandem solar cell is by connecting a large number of solar cells in parallel. Figures 6.4 and 6.5 show a schematic diagram and an energy band diagram

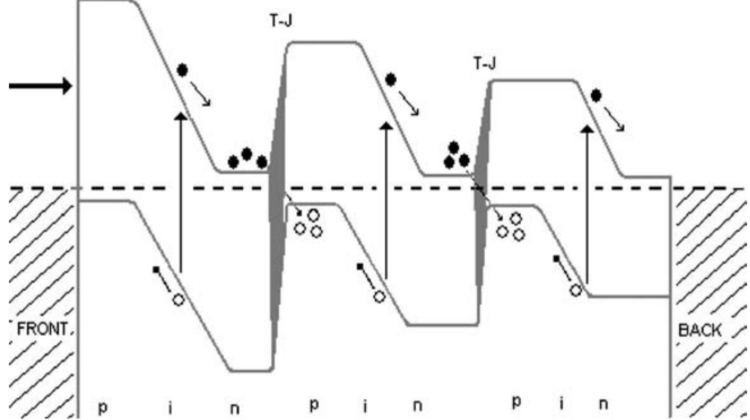

Figure 6.3 An energy band diagram of the tandem solar cell shown in Fig. 6.2, containing three p-i-n diodes.

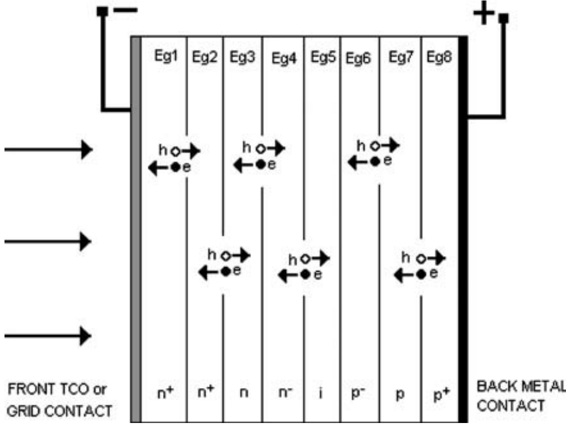

Figure 6.4 A schematic diagram of a tandem solar cell fabricated by connecting a large number of cells in parallel. The bandgaps of material layers gradually reduce ($E_{g1} > E_{g2} > \ldots > E_{g7} > E_{g8}$), and the conduction type varies from n^+ to p^+ from the front to the back of the solar cell. See also Colour Insert.

of such a device, respectively. In this case, the material changes its conduction type from n^+ to p^+ through a series of layers consisting of n^+, n, n^-, i, p^-, p and p^+. In this notation, n^+, n, n^-, and i denote heavily n-doped, moderately n-doped, low n-doped, and intrinsic

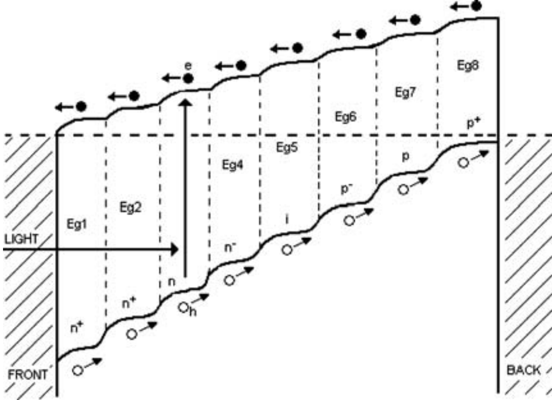

Figure 6.5 An energy band diagram of the tandem solar cell shown in Fig. 6.4. The number of semiconductor layers included in this structure is eight, including an n^+-type window material.

semiconducting materials, respectively. A similar definition applies to p-type materials, and similar structures could be built starting from p^+-type wide-bandgap materials. In this situation, the whole structure can be sliced into a large number of different solar cells, such as n^+-n-n^-, n^--i-p^-, and p^--p-p^+. The individual solar cells are connected to form a tandem solar cell. The conduction band of one device is connected to the conduction band of the adjacent device; hence, the connection is parallel. Full absorption of the solar spectrum can be achieved by gradually reducing the bandgap from the front to the back of the solar cell, as shown in Fig. 6.5. However, the lowest bandgap material used is a compromise since the open circuit voltage produced by the device depends on the minimum bandgap material used in the structure.

6.3 Comparison of the Two Connecting Methods

The two methods of connecting individual solar cells to make tandem solar cells have their advantages and disadvantages. These are discussed in detail in the following two sections.

6.3.1 *Disadvantages of Series Connections*

A tandem solar cell connected through tunnel junctions has a severe disadvantage, as shown in the energy band diagram (Fig. 6.3). The photo-generated electrons of one cell are brought closer to the photo-generated holes of the adjacent cell. These carriers are slowed down at the interface due to the existence of an internal electric field acting in the opposite direction. This increases the recombination of carriers at this interface through the tunnel junction. Figure 6.3 shows the equilibrium situation under illuminated conditions and the short circuit mode showing the direction of flow of photo-generated charge carriers. Under illumination, the device structure is equivalent to a forward-bias situation by a voltage V_{oc}. This is a supporting condition for increased recombination, and the separation of photo-generated charge carriers is severely hampered by the tunnel junction. The efficiency is reduced since conditions are created within the solar cell that promote recombination of photo-generated charge carriers without allowing them to flow through the external circuit. An animation of the working of this device can be found in Dharme's blog at www.apsl.org.uk. In this case, photons create charge carriers within the device, but the carriers killed within the device before they are separated and transported through the external circuit. Although light harvesting is effective, charge carrier separation and collections are severely hampered.

Ideally, the electrons created should be injected into the conduction band of the adjacent cell. Instead, the conduction electrons of one cell and holes of the adjacent cell are brought towards the tunnel junction (Fig. 6.3) and slowed down at that interface due to the opposite internal electric fields present near the tunnel junction. In fact, if all three solar cells absorb an equal number of photons, the external circuit will experience only the holes produced by the front cell and the electrons produced by the back cell (Fig. 6.3). In such a situation, there is no real advantage in having more cells. Any improvements observed in the past are most likely due to improvements in the quality of the material made when numerous layers are grown on top of one another, starting from the back contact. In fact, more tunnel junctions introduced in the structure increase the number of interfaces where e-h pairs can recombine.

Such an approach, in which three or more cells are fabricated, leads to cost increase but the efficiency gains are comparatively small. In this arrangement, the V_{oc} will increase by a factor of n but the J_{sc} will reduce by the same factor, where n is the number of individual devices included in the structure. The power output will remain basically the same.

6.3.2 *Advantages of Parallel Connections*

With reference to the energy band diagram for parallel connections (Fig. 6.5), e-h pairs are generated by high-energy photons in the front layers and by low-energy photons in the back layers of the cell. The photo-generated electrons are accelerated towards the front contact, and holes are accelerated towards the back contact. In this case, the recombination process has been minimised due to the improved slope and the shape of the energy band diagram. The presence of a high internal electric field in the device enables charge carriers to achieve very high kinetic energies due to continuous acceleration across the device structure. Therefore, all of the photo-generated charge carriers have the possibility of reaching the load in the external circuit. Various other loss mechanisms, such as surface reflection, are common to both systems and, therefore, have been ignored in this discussion. Since charge carriers undergo continuous acceleration, they can even create multiple charge carriers due to impact ionisation, increasing the electric current in the device (Fig. 6.6). In series connections, charge carriers are slowed down at each tunnel junction, increasing recombination and reducing the current collection in the external circuit.

In addition, the impurity PV [1] or inter-band PV effect [2] is also built into devices that are connected in parallel. The low-energy photons at the IR end travel towards the back of the solar cell. Any semiconductor material contains a number of defect levels in the bandgap, and these levels can be utilised in this device structure to increase useful charge carriers. A combination of two IR photons could create one e-h pair in any region, and these charge carriers are well separated, accelerated, and collected in the external circuit (Fig. 6.6). Various combinations of IR photons could produce many e-h pairs using different impurity levels present in

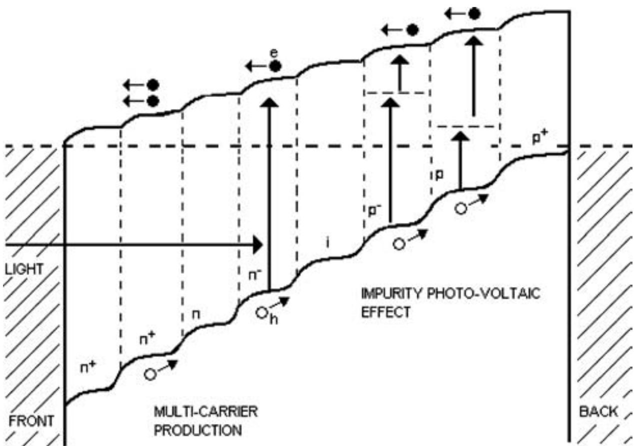

Figure 6.6 The possibility of multi-charge carrier creation by an avalanche effect and multi-step charge carrier creation using infrared (IR) photons through an impurity PV effect in tandem cells connected in parallel configuration.

the semiconductor layers, anywhere from the front to the back. This effect could also contribute to the PV activity, as shown in Fig. 6.6, enhancing the current collection from this type of device structure. The defects in semiconductors are difficult to remove — the only possibility is to minimise their concentrations. In this case, the natural defects present are used to the device's advantage rather than the detrimental recombination process. The photo-generated electrons and holes are separated by the whole device thickness, and hence recombination has been minimised. Intentionally introduced inter-bands may only be useful if they are promoting e-h pairs, by minimising the recombination process. This will be really challenging to achieve in a practical device.

The advances made in the growth of p^+, p, i, n, and n^+-type CIS and CIGS materials [3, 4] using electrodeposition are very relevant to the fabrication of multi-layer devices connected in parallel. In addition, the simultaneous bandgap engineering needed to achieve values in the range of ~2.20 to ~1.00 eV has been established [5]. By varying both bandgap and electrical conduction type, using previously described electrodeposition techniques [3–7], it is possible to fabricate device structures of the type shown in

Figs. 6.4 and 6.5. In addition, the use of electrodeposition satisfies a number of key criteria necessary for PV development, namely, its low cost, scalability, and manufacturability, ultimately contributing to increased device efficiencies and low production costs. These advantages of electrodeposition have been described in chapter 3.

6.4 Conclusions

The reconsideration of the solid-state device principles behind the fabrication of tandem solar cells allows us to draw several conclusions:

The fabrication of tandem solar cells using a series configuration, through tunnel junctions, is inefficient in charge carrier separation and collection. At each tunnel junction, photo-generated electrons and holes approach one another, are decelerated, and are allowed to recombine. The addition of more tunnel junctions is actually detrimental to charge carrier separation and collection. Any improvement observed in the device performance to date is likely due to improvements in the quality of the material achieved due to growth of a number of layers on top of one another using the most expensive and well-established metalorganic chemical vapour deposition (MOCVD) or molecular beam epitaxy (MBE) techniques. It is a remarkable achievement of nearly 40% efficient solar cells using complex device structures containing tunnel junctions — a result of three decades of research. The removal of this disadvantage from the device will lead to the formation of devices with efficiencies well above 40%.

On the other hand, the fabrication of multi-layer graded bandgap solar cells using a parallel configuration has several advantages. Variation of the conduction type from n^+ to p^+ combined with bandgap variation from high to low from the front to the back of the solar cell provides many positive results. Photo-generated charge carriers at any depth of the device are effectively separated, accelerated, and collected in the external circuit.

Continuous acceleration across the whole device thickness could produce high-speed carriers and, therefore, results in multi-charge carrier production through impact ionisation. In addition, the

impurity PV activity could also pump electrons into the conduction band using different combinations of most of the IR radiation. These e-h pairs are also effectively separated, accelerated, and collected in the external circuit, enhancing the short circuit current density of the device. The improvement in the performance of tandem solar cells will manifest itself mainly in high short circuit current densities since both open circuit voltage and fill factor values are approaching their maximum values in such devices.

The removal of tunnel junctions from tandem solar cells and the adoption of a parallel configuration will lead to high performance next-generation solar cells in the future. The initial testing of parallel configurations using GaAs/AlGaAs systems has been carried out, and the experimental results are presented in the next two chapters.

6.5 Summary

Different ways of connecting solar cell structures to effectively harvest photons in tandem solar cells have been considered by revisiting relevant device designs. It is found that the present use of a series connection or tunnel junction approach is detrimental to charge carrier separation and collection through the tandem cells. Each tunnel junction introduced to the solar cell structure decelerates the charge carriers and allows them to recombine at the vicinity of the tunnel junction. The adoption of parallel connections has several advantages over series connections, and there is high potential for achieving enhanced efficiencies in next-generation solar cells. In these devices, charge carriers are continuously accelerated across the whole device and collected in the external circuit. Multi-charge-carrier production by impact ionisation and impurity PV mechanisms are also built into this system to enhance its performance through the possibility of increasing the short circuit current density.

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Chapter 7

Multi-Layer Graded Bandgap Solar Cells

7.1 Introduction

In order to effectively harvest photons from all spectral regions (ultraviolet [UV], visible, and infrared [IR]) and combine the impact ionisation and impurity photovoltaic (PV) effects, a multi-layer graded bandgap solar cell structure was introduced in chapter 6. This structure is based on an n-type window material layer. However, improved results can be obtained from device structures starting with p-type window materials. As indicated in section 1.6 of chapter 1, these two structures are shown in Fig. 1.16. The structure with p-type window material has additional advantages over that with n-type window material. The potential barrier height (ϕ_b) for electron flow through the device structure is determined by the large bandgap of the window material. This is, therefore, capable of producing high potential barriers and, hence, large V_{oc} values. In addition, the electrons produced by high-energy photons can accelerate and create more charge carriers due to impact ionisation, because of the smaller bandgap present at the rear of the solar cell. Because of these additional advantages, the experimental testing was carried out only on this device structure with p-type window material. This chapter presents the experimental

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results achieved within only two growths using a well-researched metal organic vapour phase epitaxy (MOVPE)-grown GaAs/AlGaAs material system. GaAs/AlGaAs is the best-researched inorganic material system next to Si. The author has, therefore, purposely selected this well-explored system to test this new design proposed for PV solar cells.

7.1.1 *Incorporation of Impurity PV Effect*

In real semiconductors, there are many defect levels present due to impurities and native defects. It is also natural to have more energy levels close to the growth substrate due to lattice mismatch and other surface effects. In this device structure (Fig. 7.1), these impurity levels exist close to the rear of the device, where the growth has started from a GaAs substrate, and are used to convert IR photons into useful charge carriers. Absorption of two or more IR photons at different absorption stages could create one e-h pair. In these events, holes in the valence band and the electrons in the conduction band appear at two different times and are readily separated by the effective slopes available throughout the device. This process reduces the probability of detrimental recombination of e-h pairs due to defects in the device. This new design, therefore,

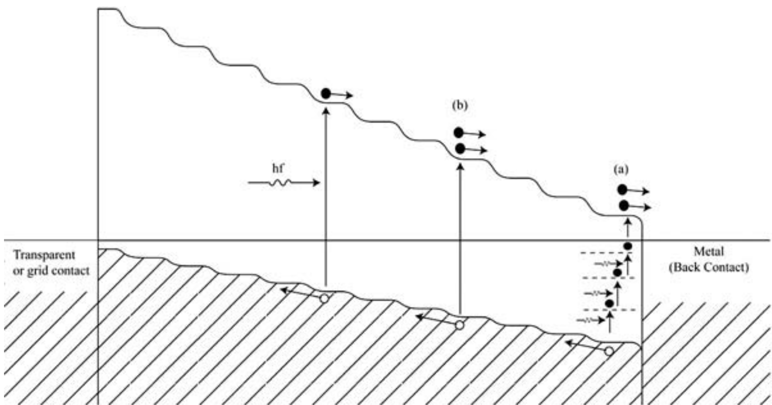

Figure 7.1 A new design proposed for PV solar cells to maximise optical absorption and minimise thermalisation and transmission losses by combining the impurity PV effect and impact ionisation.

makes use of the naturally occurring defect levels to create more charge carriers using the impurity PV effect, reducing the competing recombination and generation (R&G) process. It is important to note that in this structure, the photo-generated charge carriers are separated by the whole thickness (about 3 μm) of the active solar cell structure and, hence, the probability of R&G process has been further reduced.

7.1.2 *Incorporation of Impact Ionisation*

There is another mechanism of charge carrier creation incorporated in this device structure. The electrons excited into impurity levels by IR photons can be promoted to the conduction band by either using another IR photon or by impact ionisation. The electrons created by UV and visible photons at the front of the device [1] accelerate through the structure, gaining adequate momentum to knock off electrons trapped in defect levels at the rear, into the conduction band — process (a), Fig. 7.1. The transmission losses are, therefore, reduced through the combination of IR excitation of electrons to defect levels and promotion of these electrons to the conduction band by impact ionisation. Photo-generated electrons created at the front of the device may also acquire enough energy to break another bond — band-to-band transition, as shown by process (b), Fig. 7.1 — close to the back contact of the device due to a smaller bandgap present in this region of the solar cell. Therefore, impact ionisation could help in two different ways to create more charge carriers in this device.

The composition grading adds ~0.70 V to the voltage difference across the device due to the grading over 3 μm thickness. This corresponds to an enhancement of internal electric field by ~2.30 $kVcm^{-1}$. This additional electric field will enhance the charge separation and the impact ionisation process in these devices.

7.2 Summary of Growth and Process Details of the Device Structure

A device structure with an energy band diagram as shown in Fig. 7.1 was first fabricated using the GaAs/AlGaAs system grown by the

MOVPE technique. The full design, growth, and process details have been described in publications in 2005 and 2006 [2–4]. The graded bandgap device structure was grown starting from an n^+-GaAs substrate by incorporating increasing amounts of Al into the material. The total device thickness was restricted to $\sim$3 μm, and the material structure was capped with a 0.2 μm p-GaAs layer in order to prevent the oxidation of Al in the layer before processing of devices. The material layers at the back of the solar cell were doped with Si to make the material n-type in electrical conduction. The doping concentration was gradually reduced to form i-type material in the middle of the cell structure. The material layers towards the front of the cell were doped using background C by controlling the growth temperature. The aim was to gradually convert the material layers from i-type to p-type electrical conductivity from the middle to the front of the device, forming an overall graded bandgap p-i-n type device structure.

The two electrical contacts, at the front (Ti/Au grid contact) and the back (In/Ge + Au), were fabricated using established technologies in order to achieve low resistance ohmic contacts [5–7]. The reflection losses have been minimised using SiN_x- and MgF_2-based anti-reflection coatings. This structure, when fabricated with all required features shown in Fig. 7.1, maximises the absorption of solar radiation, minimises thermalisation effects, separates photo-generated charge carriers swiftly, and passes these through to the external circuit efficiently in order to create useful output power.

7.3 Experimental Results of Fully Processed Devices

Solar cells of different sizes — 0.5 mm diameter, 3×3 mm^2, 5×5 mm^2, and 10×10 mm^2 — were fabricated for device characterisation and to check the effect of a gradual scaling up of the device. The capping layer of 0.2 μm p-GaAs was completely removed by chemical etching during device processing. Figure 7.2 shows the four different sizes of devices processed. The assessment results of these solar cells are summarised in the following sections.

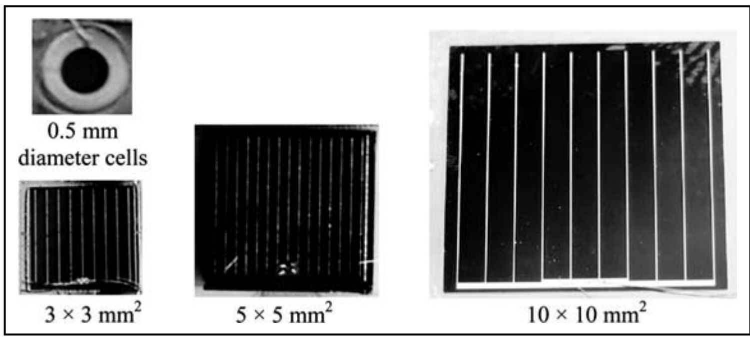

Figure 7.2 A photograph of solar cells fabricated with different dimensions to test the effects of the scaling-up process. See also Colour Insert.

7.3.1 *Electrical Properties Under Dark Conditions*

The dark current-voltage (I-V) curves of these devices show excellent rectification properties. The breakdown voltages in the reverse-bias mode extend beyond 45 V, showing the strength of the rectifying structures. The ideality factors (n) vary in the range 1.41–2.26, and the ϕ_b values estimated using I-V curves with the lowest values of n are greater than 1.60 eV (see Table 7.1). The accuracy of ϕ_b depends on the value of n and, therefore, the conclusion made by these measurements is that the potential barriers that exist in these devices are greater than 1.60 eV. These values of n indicate the presence of the R&G mechanism in the current conduction process under dark conditions even in these epitaxially grown materials [7]. This highlights the effects of the R&G process on devices, fabricated

Table 7.1 Typical values of n and ϕ_b measured under dark conditions

	Device Parameters	
Diode Number	***n***	**ϕ_b (eV)**
1	1.41	>1.60
2	1.50	>1.56
3	1.68	>1.48
4	1.84	>1.43
5	2.26	>1.27

with even the best semiconductor growth technique and improved device structure. Even with highest internal electric field available, the recombination process cannot easily be minimised due to the presence of active R&G centres. The presence of high potential barriers indicates the possibility of achieving large V_{oc} values from these structures since V_{oc} is a function of ϕ_b, as given by Eq. 1.16.

The capacitance of the 0.5 mm diameter devices was also measured at 1 MHz frequency, as a function of the DC bias voltage. Mott-Schottky graphs were plotted in order to estimate the doping concentration of the material layers at the edge of the depletion region. A typical $1/C^2$ versus V plot, shown in Fig. 7.3, indicates an arc instead of the usual straight line observed for devices with a uniform doping concentration. The doping concentration at the edge of the depletion region at zero bias is 4×10^{17} cm^{-3}, and this value shows a gradual change as the DC bias is applied to the device structure. This gradual change of doping concentration is expected from this device structure since it was intentionally introduced to the system.

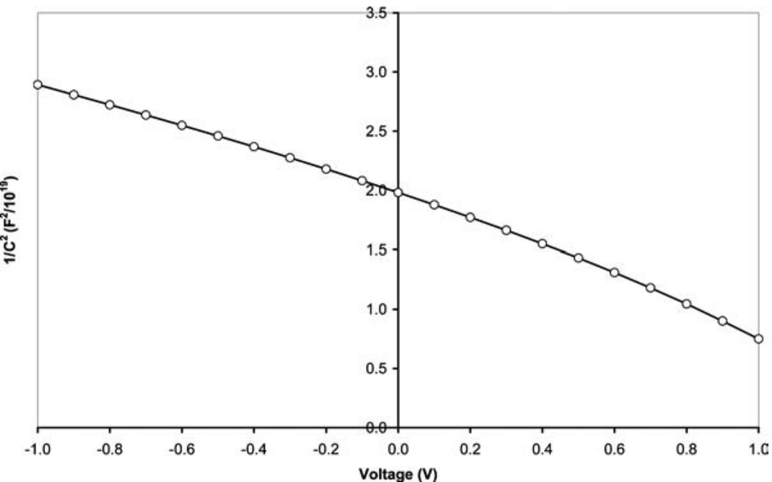

Figure 7.3 A typical Mott-Schottky plot observed for graded bandgap devices, showing a gradual change in the doping concentration, as expected for this device.

Table 7.2 Typical values of n and ϕ_b measured under dark and illuminated conditions

	Under Dark Conditions		**Under AM1.5 Illumination**	
Diode Number	n	ϕ_b **(eV)**	n	ϕ_b **(eV)**
1	1.41	>1.60	1.13	>1.79
2	1.50	>1.56	1.15	>1.70
3	1.68	>1.48	1.22	>1.70
4	1.84	>1.43	1.14	>1.76
5	2.26	>1.27	1.91	>1.34

7.3.2 *Electrical Properties Under AM1.5 Illumination*

The rectification properties of these devices improve under air-mass 1.5 (AM1.5) illumination. The values of n estimated from I-V curves under illumination vary in the range 1.13 to 1.91, indicating a considerable reduction of the R&G process under illumination (see Table 7.2). This data indicates that most of the defects have reduced R&G activities under illuminated conditions. Since the values of n are close to unity, barrier heights can be estimated with an improved accuracy. These measurements indicate that the ϕ_b values for these devices are greater than 1.79 eV.

The linear-linear I-V curves observed under AM1.5 illumination exhibit excellent PV properties and a typical curve is shown in Fig. 7.4. This device shows PV parameters; $V_{oc} = 1,171$ mV, $J_{sc} = 12$ mAcm^{-2}, and fill factor (FF) $= 0.85$ with an overall efficiency of $\sim$12%.

Table 7.3 presents a summary of PV parameters measured at different laboratories for different devices processed from one batch. The V_{oc} values observed are in the range 1,141–1,171 mV, as expected from devices with high ϕ_b values. These device parameters have been independently verified by measuring in five different laboratories, and the PV parameters show similar values, confirming the accuracy of measurements. These V_{oc} values exceed the highest reported values to date [8, 9] for a GaAs/AlGaAs single-device system. Furthermore, these parameters hold when the area of the device is increased to 5×5 and 10×10 mm^2. This is expected since the uniform epitaxial material layers are grown by the well-established MOVPE technique.

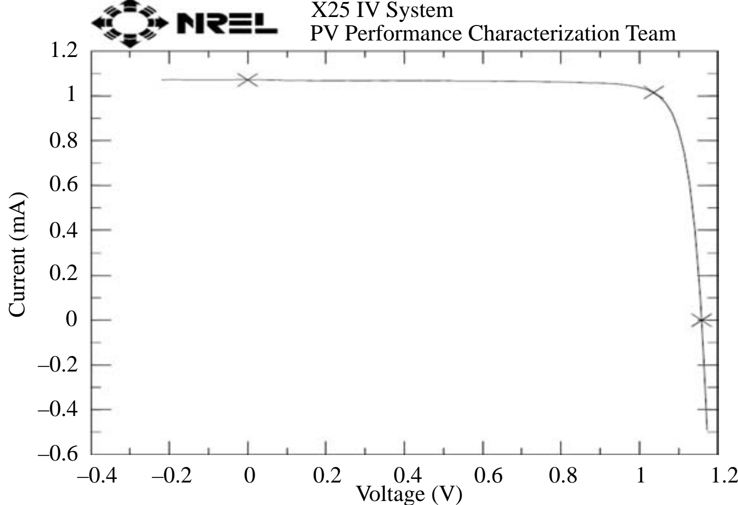

Figure 7.4 A typical I-V curve measured under AM1.5 illumination for a 3×3 mm^2 graded bandgap multilayer GaAs/AlGaAs solar cell showing $V_{oc} = 1,171$ mV, $J_{sc} = 12$ mAcm^{-2}, FF = 0.85, and $\eta = \sim 12\%$.

Table 7.3 A summary of solar cell parameters measured at five different laboratories for 3×3 mm^2 graded bandgap solar cells processed in one batch

Device	V_{oc} (mV)	FF	J_{sc} (mAcm^{-2})	R_s (Ωcm^2)	R_p (Ωcm^{-2})	Place of Assessment
1	1,170	0.87	—	—	—	SHU Labs
2	1,160	0.86	—	—	—	Dharmadasa *et al.*
3	1,148	0.86	10.7	2.5	10,400	Zürich Labs
4	1,141	0.86	10.3	4.0	5,100	Tiwari *et al.*
5	1,169	0.85	11.5	—	—	SBU Labs
6	1,149	0.86	10.0	—	—	Reehal *et al.*
7	1,150	0.85	12.1	3.8	—	EPFL Labs Grätzel *et al.*
8	1,159	0.85	12.3	—	—	NREL, US
9	1,171	0.85	12.0	—	—	Gessert *et al.*

It is noteworthy that during measurements, V_{oc} values of 1,180, 1,195, and 1,205 mV have also been observed. This is a typical behaviour of electronic devices and a strong indication of the possibility of V_{oc} exceeding a key milestone, 1,200 mV, for these devices, with

further improvements. 1,200 mV is the minimum voltage required to split water molecules using electrolysis.

The FF values measured for these devices are achieving the maximum possible value for this parameter. FF values remain in the mid-80% range, and the highest value recorded was 0.87. These values are holding for 0.5 mm diameter, 3×3 mm^2, 5×5 mm^2, and 10×10 mm^2 size solar cell devices without any reduction during the gradual scaling-up process. These reproducible results indicate that the losses due to series resistance and shunt resistance are at their lowest for these device structures and hence the maximum possible FF values have been achieved.

7.3.3 *IPCE Measurements*

The current density values measured for these devices are in the range 10–12 mAcm^{-2}. These values are very low for devices based on GaAs/AlGaAs systems when compared to the capability of these materials and the new device structure. To explore the reasons for these low current density values, incident photon to current conversion efficiency (IPCE) measurements have been carried out on these devices. Measurements of IPCE of several devices showed a considerable loss in both blue and red regions. A typical example is shown in Fig. 7.5.

One explanation for this severe loss is the remains of the 0.2 μm thick p-GaAs used as a capping layer. Tests have been carried out to make sure the capping layer was completely removed during chemical etching. Although the p-GaAs capping layer is completely removed, the shape of the IPCE remained the same, indicating the existence of another reason causing these losses. This conclusion led to the use of the electron beam–induced current (EBIC) technique to further explore the possible causes.

7.3.4 *EBIC Measurements*

Cross-section EBIC experiments have been carried out on these devices to investigate the PV-active region across the device thickness. Figure 7.6 shows a typical EBIC-line spectrum and an EBIC image for this device structure. According to these measurements, the width of

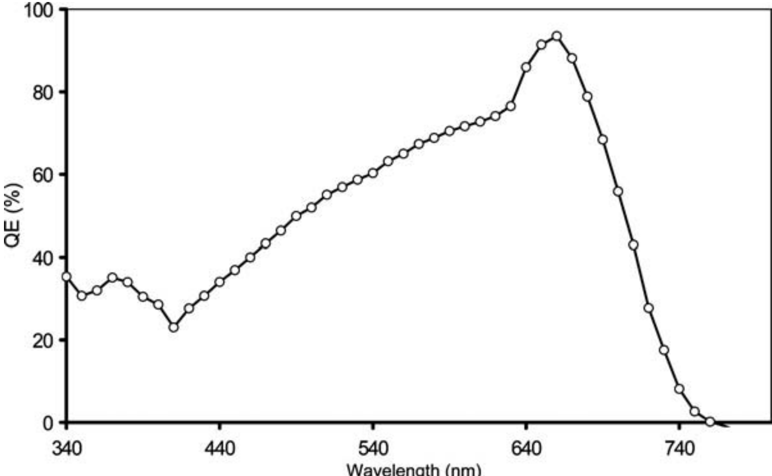

Figure 7.5 A typical IPCE curve measured for a 3 × 3 mm^2 solar cell. Note the severe losses at the blue end and close to the GaAs cut-off wavelength of ~855 nm.

the depletion region is ~1.50 μm and starts from ~0.87 μm from the front surface.

This experimental evidence indicates that although the desired device design was as shown in Fig. 7.1, during the first MOVPE growth of the materials, only a 1.50 μm thick depletion region has been formed within the device. The thickness of 0.87 μm to the front and 0.83 μm to the back of the device remains at nearly flat-band conditions due to high doping levels (see Fig. 7.7). The slight slopes available are due to the bandgap grading in these two regions. The ideal situation would be to have a ~3 μm thick depletion region to cover the full width of the device. This observation invoked the study of doping concentration using secondary ion mass spectroscopy (SIMS) profiling through the device structure.

7.3.5 *SIMS Profiling*

A sample of the same wafer has been used for depth profiling by SIMS at Loughborough Surface Analytical Ltd. A typical profile is shown in Fig. 7.8 for this device structure. The C and Si profiles were quantified (left-hand scale), whereas the Al and As profiles were

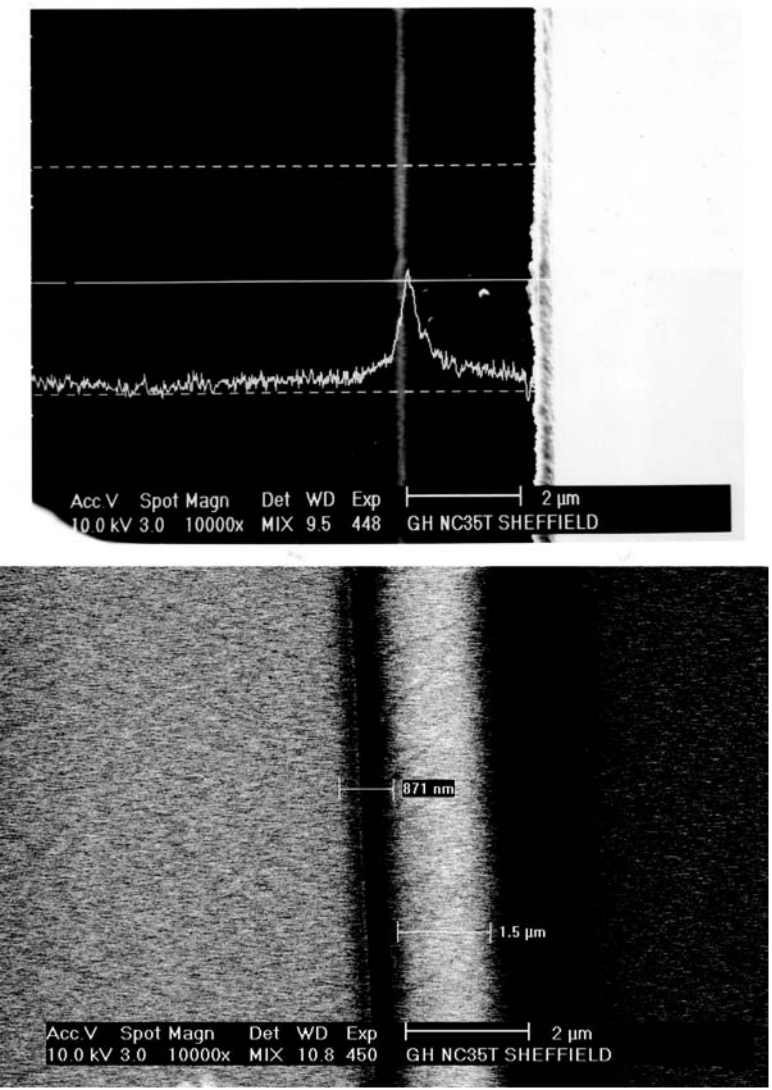

Figure 7.6 An EBIC line graph and EBIC image of the cross-section of the GaAs/AlGaAs solar cell showing PV activities across the width of the device.

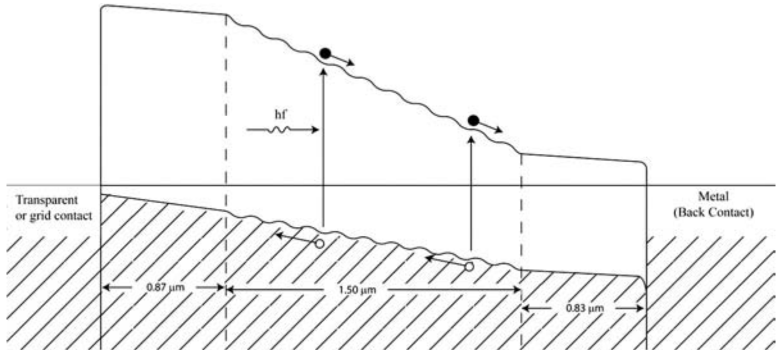

Figure 7.7 A band diagram of the device fabricated during first growth due to high doping concentrations at both ends of the structure.

unquantified (right-hand scale) in this graph. As expected, the As concentration remains constant throughout the structure and the Al concentration gradually increases towards the front of the device. The termination of the Al signal at 3.2 μm from the front surface produces an approximate value for the thickness of the solar cell. A peak on the C signal also coincides with this value, confirming

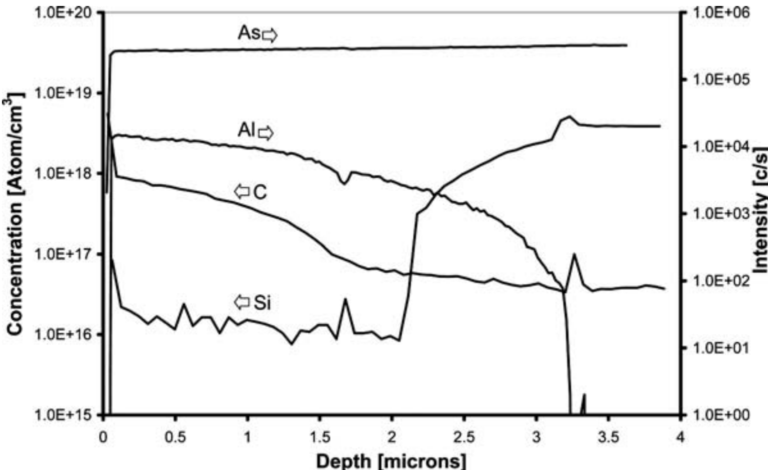

Figure 7.8 A typical SIMS depth profile through the AlGaAs/GaAs solar cell showing high doping concentrations, of about 10^{18} cm^{-3}, for n-type (Si) and p-type (C) dopants.

the starting position of the MOVPE-GaAs growth surface. The Si and C doping concentrations are the key parameters that control the depletion width of the solar cell device.

It is evident that the Si doping at the back end of the solar cell starts from $\sim 6 \times 10^{18}$ cm^{-3} and gradually reduces as expected. In the front end, the background C doping has also increased to $\sim 1 \times 10^{18}$ cm^{-3}. These results indicate that the doping concentrations at both ends are too high and, therefore, should be reduced to the range $\sim 5 \times 10^{14}$ to $\sim 5 \times 10^{15}$ cm^{-3} levels to extend the depletion region to ~ 3 μm [10]. As the next improvement step, it is clear that the reduction of n doping at the back end and p doping at the front end of the cell is needed. As a result of these high doping concentrations, the band diagram of the device fabricated during the first attempt is as shown in Fig. 7.7 instead of the expected band diagram, as shown in Fig. 7.1. The MOVPE method is capable of reducing the n doping (Si) only at the back end, and not the doping due to background C at the front end. Therefore, the second growth run was mainly aimed at reducing Si doping to a lower level.

7.3.6 *Optimisation of Si Doping Concentration*

The experimental results presented above were achieved during the first growth run. A second growth was carried out to reduce both Si doping and C doping to a lower level. However, in this case, only Si doping could be reduced at the back of the device. Although it is difficult to control the background C doping at the front of the solar cell using the MOVPE method, the following steps were also taken to reduce the C incorporation in the layers.

The C residue associated with MOVPE-grown AlGaAs is strongly dependent on substrate orientation. For (100) GaAs with a 3° off to [110] orientation, there is a minimum C fraction of approximately 1×10^{16} cm^{-3}. The GaAs wafer with this orientation was, therefore, used in the second growth in the hope of minimising C incorporation.

The device structures grown on a different GaAs substrate using low Si doping produced I-V curves shown in Fig. 7.9. There are two main observations from these measurements. The improvement of J_{sc} to ~ 24 mAcm^{-2} and the overall efficiency to 18.6% (see

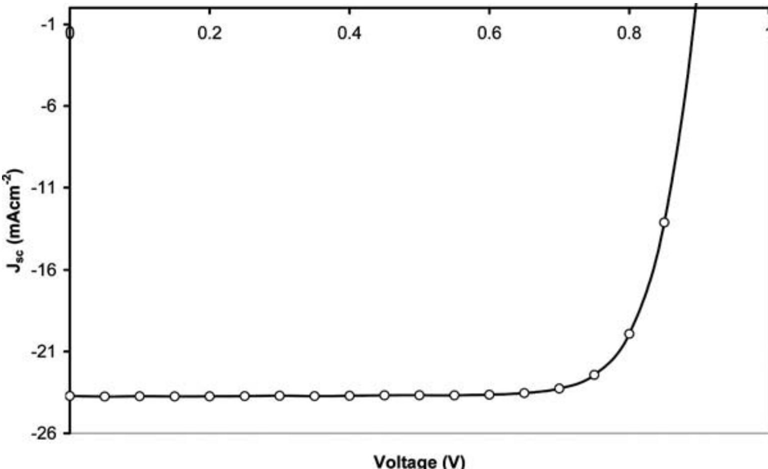

Figure 7.9 An I-V curve under AM1.5 illumination, after lowering the Si-doping concentration at the rear of the solar cell showing $V_{oc} = 900$ mV, $J_{sc} = 24$ mAcm^{-2}, FF = 0.86, and conversion efficiency (η) = 18.6%.

Table 7.4 Improvement of device parameters after the reduction of n doping with Si at the back end of the solar cell

Device Parameter	Values from the First Growth	Values from the Second Growth
V_{oc} (mV)	$1{,}156 \pm 15$	~900
FF	0.86 ± 0.01	0.86
J_{sc} (mAcm^{-2})	11.1 ± 1.1	24.0
η %	11.0 ± 0.8	~18.6

Table 7.4). These devices also showed an unexpected reduction in V_{oc} to ~900 mV instead of $1{,}156 \pm 15$ mV, as observed before for the first growth.

As expected, the IR end of the IPCE has been drastically improved with an enhanced J_{sc} from ~12 to ~24 mAcm^{-2} (see Fig. 7.10). The cut-off wavelength has shifted from ~740 (see Fig. 7.5) to 855 nm, as expected, improving the collection at the back end. The collection at the UV end, however, has not improved, indicating the non-reduction of C doping.

These experimental observations confirm that the lowering of Si doping has achieved the expected changes to the energy band

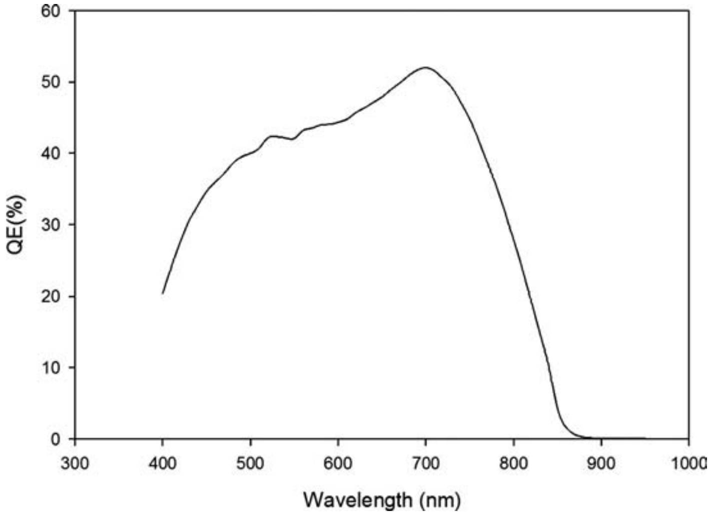

Figure 7.10 An IPCE curve measured for 3 × 3 mm^2 solar cells after reducing Si doping at the back of the solar cell. Note the drastic improvement at the IR end showing 855 nm GaAs cut-off wavelength instead of 740 nm, as shown in Fig. 7.5.

diagram. The situation for this case is now shown in Fig. 7.11, and the rear section of the solar cell has achieved the required shape due to lowering of Si doping. Therefore, the spectral response has improved at the IR end, showing the right cut-off wavelength of 855 nm (corresponding to the bandgap of GaAs) instead of

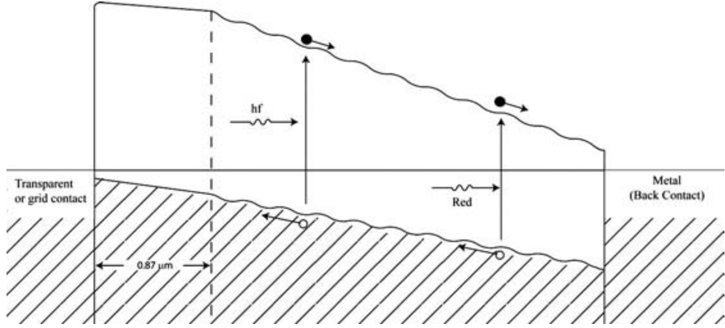

Figure 7.11 An energy band diagram of the improved device with lower Si doping at the rear of the solar cell.

740 nm, as observed before. The increase in J_{sc} value from 12 to 24 $mAcm^{-2}$ highlights the expected results from this improved device.

The third stage is, therefore, to optimise the doping concentration at the front end of the device, and this must be carried out using a molecular beam epitaxy (MBE) technique. The MOVPE method cannot control the background C doping to improve the collection of charge carriers created by UV and visible light. Since the built-in electric field is weak in the front region of $\sim$0.87 μm, the optimisation (reduction of C doping to $\sim 5 \times 10^{14}$ to $\sim 5 \times 10^{15}$ cm^{-3}) of C doping will show a further improvement of J_{sc}. The contribution arising from the IR end is comparatively small due to the low density of photons available in the solar spectrum. However, when the doping concentration in the front is optimised, the contribution to the current density should increase considerably due to the presence of a large number of photons in the visible region of the solar spectrum. The GaAs-based p-n junction devices have produced J_{sc} values of $\sim$40 $mAcm^{-2}$ [11]. The device structures described in this chapter exploiting graded bandgaps, impact ionisation, and impurity PV effect could, therefore, produce current densities well beyond 40 $mAcm^{-2}$. This means that these devices, once optimised, could easily achieve efficiencies above 40% (V_{oc} =$\sim$1,170 mV, FF =$\sim$0.85, and $J_{sc} >$ 40 $mAcm^{-2}$). Here lies an opportunity for an expert MBE grower to test this third, and final, stage and produce a high-efficiency solar cell device. A similar device structure based on InGaN alloy system could even achieve better results with this approach.

The I-V curve shown in Fig. 7.9 also indicates the possibility of Fermi-level pinning in GaAs-based solar cells. The second growth in this series used a GaAs wafer with a different crystal orientation to that of the first wafer. These devices showed V_{oc} $\sim$900 mV instead of expected $V_{oc} = 1,156 \pm$ 15 mV. This vast difference is clearly due to a different potential barrier present within the device. The independent research by Bauhuis *et al.* [11] has also shown the production of V_{oc} values in two different bands, 830–880 mV and 1,010–1,040 mV. This raises the question of whether the Fermi-level pinning is equally valid for GaAs-based solar cells, similar to those observed for CdTe [12–15] and CIGS-based solar cells [16, 17]. This subject is briefly described in chapter 11, since the experimental evidence is appearing to indicate a similar trend.

7.4 Discussions

This chapter has been devoted to presenting the advances made with a new device structure for PV solar cells. Its performance has been experimentally explored using a well-researched GaAs/AlGaAs system. Thermalisation losses have been minimised using a graded bandgap multi-layer solar cell structure. By starting with a large bandgap material in the front and a gradual reduction of the bandgap towards the back of the solar cell, a major part of the solar spectrum can be absorbed while reducing thermalisation losses. This approach has a cooling effect for the solar cell with effective absorption of the major part of the solar spectrum and the creation of enhanced charge carriers.

This multi-layer graded bandgap device structure also utilises a major part of IR radiation, minimising transmission losses. Close to the back end of the solar cell, the abundance of naturally occurring defects plays a very useful role in creating e-h pairs, combining impurity PV effect and impact ionisation, in addition to taking part in the detrimental R&G process. Although the defects take part in two competing processes, R&G has been suppressed to a certain extent and the impurity PV effect has been enhanced by the shape of the device structure. The carriers are readily accelerated and separated by the slope of the device, and photo-generated carriers are kept away from each other (see Fig. 7.12), reducing the recombination even further. The defect levels present at different depths take part in pumping electrons to the conduction band through the impurity PV mechanism. These defect levels also combine impurity PV and impact ionisation due to accelerated electrons in the conduction band to create more e-h pairs using IR radiation. Therefore, this is an excellent way of reducing transmission loss by converting the presence of defects into the device's advantage.

Finally, the losses due to both series and shunt resistance have also been minimised. The series resistance due to materials have been minimised by growing epitaxial layers with the well-established MOVPE method, and the contact resistance has been minimised by using well-established low resistance front and back contacts to AlGaAs and GaAs [6, 5]. The leakage resistance has been maximised by minimising leakage paths using epitaxial material layers.

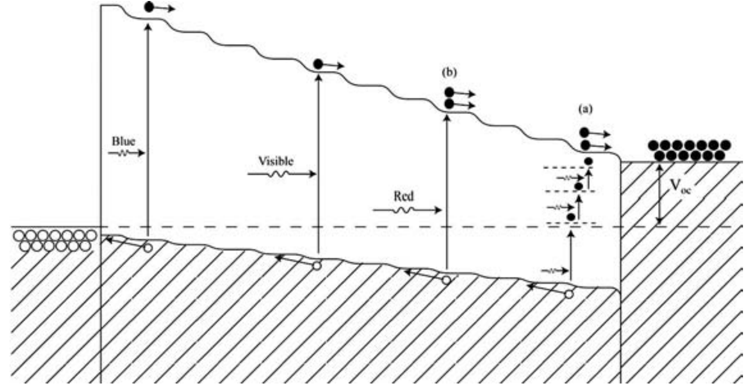

Figure 7.12 An energy band diagram of a solar cell under illumination and open circuit condition. Note the reduced R&G process by separating photo-generated charge carriers by the ~3 μm solar cell device thickness.

The expected improvements have been experimentally demonstrated by producing the highest V_{oc} = 1,141–1,171 mV values with the largest possible FF = 0.85–0.87 values. The current density values were low due to undesirable doping concentrations in the front as well as back ends of this device. The n-type Si doping concentration has been reduced using MOVPE, demonstrating a substantial improvement in J_{sc}, increasing from ~12 to 24 mAcm^{-2}, and the improved IPCE spectrum is shown in Fig. 7.10. But the p-type doping concentration cannot be adjusted using this growth technique. The MBE growth technique is the right method to achieve low C-doping levels in the front of the device, to observe the next drastic improvement.

It is anticipated that high current density values are obtained after the reduction of p-type doping to ~5×10^{14} to ~5×10^{15} cm^{-3} levels in the front layers. There are many other possible improvements that could be introduced to this device structure for further development. These include matching of semiconductor layer thicknesses to the solar spectrum in order to improve the effective light absorption and the modification of electrical contacts, including the electron back diffusion barrier (ebdb) and hole back diffusion barrier (hbdb) layers at both ends, as reported in papers published in 2009 [16, 17].

7.5 Summary

A solar cell design based on p-type window materials has been used to minimise loss mechanisms and achieve high performance parameters in solar cells. This design has been experimentally tested using the well-researched GaAs/AlGaAs system, grown by the MOVPE method. Device parameters were assessed in different laboratories using I-V and incident photon to current conversion efficiency (IPCE) measurements. Independently verified device parameters of $V_{oc} = 1{,}141–1{,}171$ mV, $J_{sc} = 10–12$ mAcm^{-2}, and FF $= 0.85–0.87$ have been achieved for initial devices. The overall efficiency values measured for devices of different sizes — 0.5 mm diameter contacts and 3×3, 5×5, and 10×10 mm^2 — were in the range of 11–12%. The V_{oc} achieved in this work exceeds reported values in the literature, and FF values have reached their maximum possible values in the mid-80% range. EBIC and SIMS measurements revealed the reasons for the low J_{sc} values. It has been found that the doping concentrations at both front and back ends of the device were too high, producing partially depleted devices for the first growth run. The reduction of doping concentration at the back end of the device improved the short circuit current density from $\sim$12 to $\sim$24 mAcm^{-2}, improving the efficiency to 18.6%. Considerable improvements in J_{sc} and, hence, the overall efficiency are anticipated by optimising p-doping concentrations at the front end of the device structure. This chapter invites an MBE grower to reduce the p-type doping concentration to $\sim 10^{15}$ cm^{-3} in the front of the device, which cannot be achieved by the MOVPE method. The work also opens doors for InGaN alloy-based graded bandgap devices to achieve very high efficiencies. This optimisation could yield a considerable improvement of the overall efficiency of this device.

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Chapter 8

Solar Cells Active in Complete Darkness

8.1 Introduction

Traditionally, solar radiation is exploited using two different methods, solar thermal technology using infrared (IR) radiation and photovoltaic (PV) technology using visible and ultraviolet (UV) radiation. In order to be cost effective, it is attractive to combine both together in one device. In addition, if the incorporation of phenomena such as impact ionisation and impurity PV can be built into the same device, the performance of a solar cell can be enhanced. With these aims in mind, a graded bandgap multi-layer device structure has been designed and experimentally tested with a well-researched GaAs/AlGaAs system. Design details and experimental results are presented in chapters 6 and 7. This chapter presents the experimental evidence observed for the impurity PV effect expected from these device structures.

8.2 Summary of Experimental Results

The device design proposed for the combination of all the above features is presented in chapter 6, and the details are published

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elsewhere [1–4]. The four most important steps for an efficient solar cell are satisfied for this structure (Fig. 7.1) according to solid-state physics principles, namely (i) the absorption of a major part of the solar spectrum, (ii) the creation of e-h pairs in the presence of an internal electric field, (iii) the effective separation of charge carriers towards two electrical contacts and (iv) transport through an external electric circuit. Because the device starts from a large bandgap p-type semiconductor and is completed with a narrow bandgap n-type semiconductor, the probability of impact ionisation and the impurity PV effect has been increased. The detailed working of this device is illustrated with an animation placed on the website Dharme's blog at www.apsl.org.uk (Tunnel Junction File).

The first growth of this device structure was made using metal organic vapour phase epitaxy (MOVPE)-GaAs/AlGaAs materials. The devices exhibited $V_{oc} = 1{,}150$–$1{,}175$ mV, $J_{sc} = 10.3$–12.3 mAcm^{-2}, fill factor (FF) $= 0.85$–0.87, and conversion efficiency (η) $= 11$–12%. It is worth noticing the achievement of the highest-reported V_{oc} for a single device [5, 6] together with the highest achievable FF values. These parameters were independently verified by measuring in five different laboratories in Europe and United States, including National Renewable Energy Laboratory (NREL).

Attempts made to improve the current density were presented in chapter 7. During this second growth, the $V_{oc} = 900$ mV, $J_{sc} = 24$ mAcm^{-2}, FF $= 0.86$, and $\eta = 18.6\%$ values were observed with additional information. The variation of V_{oc} is noteworthy, and the new information emanating for GaAs-based solar cells is summarised in chapter 11. The overall conversion efficiency for the graded bandgap multi-layer solar cell has improved from $\sim$12% to 18.6% during the second attempt.

8.3 Search for Experimental Evidence of the Impurity PV Effect

The device structure shown in Fig. 1.16 was designed to incorporate impurity PV effect using native defects available closer to the GaAs substrate at the back of the device. The experiments were, therefore,

performed in order to test the existence of this effect in these devices. The most relevant technique is the quantum efficiency (QE) measurement to test whether there is a collection of current in the IR region. There are two types of QE measurements used in solar cell assessment, external QE and internal QE. External QE measurements include the effects of optical losses, such as transmission through the cell and reflection from the surface. Internal QE refers to the efficiency with which photons that are not reflected or transmitted from the cell can generate collectable charge carriers. Internal QE is also referred to as incident photon to charge carrier efficiency (IPCE), and this is the method used to measure the graded bandgap multi-layer solar cells.

Figure 8.1 shows the IPCE measurements carried out for two devices in two different laboratories. Their features are similar, and the losses at UV and IR ends are due to high doping of the materials at both front and back of the cell. These issues are described in chapter 7 and dealt with separately in order to achieve the full features shown in Fig. 1.16 and increase the performance of the

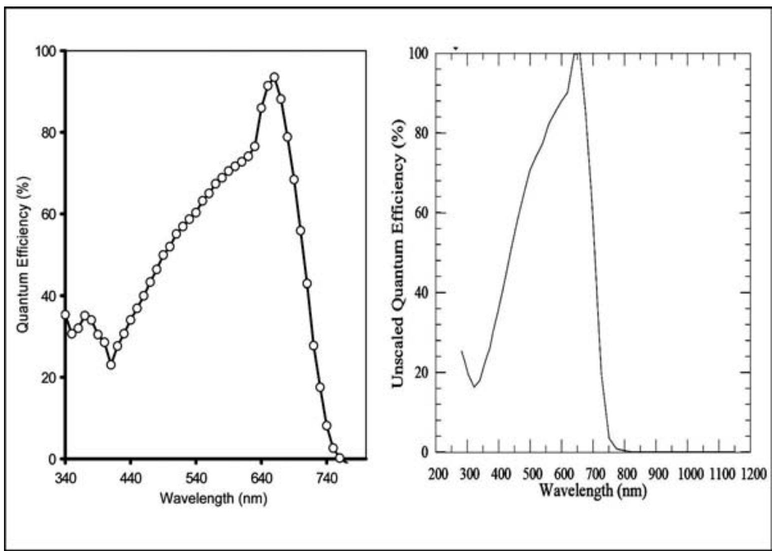

Figure 8.1 Typical IPCE% curves measured for two 3×3 mm^2 solar cells. Note the sharp cut-off wavelength at $\sim$740 nm indicating a null collection in the IR region.

device structure. The aim of this work is to experimentally observe whether the impurity PV effect is contributing to charge carrier creation in these devices. The IPCE measurements show a sharp cut-off at ~740 nm, indicating that there is no collection in the IR region. According to these measurements, there is no contribution from the impurity PV effect in these devices.

8.4 Responsivity Measurements

The above measurements clearly raised an issue of disagreement between the theoretically expected impurity PV effect and the experimentally observed null results. This encouraged the re-examination of the ways of data collection, analysis, and presentation of IPCE results, and it was found that there are grey areas which are not clear to the experimentalists. For this reason, a straightforward measurement of responsivity as a function of wavelength was explored. The responsivity of a device is defined as:

$$\text{Responsivity (A/W)} = \text{Electrical output of the solar cell (A)} / \text{Light input to the solar cell (W)}$$

This method is fully transparent to the experimentalist and removes all complications in data collection, analysis, and graphical presentation. The two required parameters, light input and the current output, are measured and plotted directly without further processing of experimental data.

Figure 8.2 shows a typical measurement, and the main spectrum shows similar losses in UV and IR ends as observed in IPCE measurements. However, the collection in the IR region, up to ~1,200 nm, is clearly observed in these measurements. This is a strong indication that during IPCE data collection, analysis, and graphical presentations, this useful information is completely lost.

8.5 I-V Measurements Under Dark Conditions

The positive indication of existence of impurity PV effect encouraged further investigation of this effect using other techniques. The most

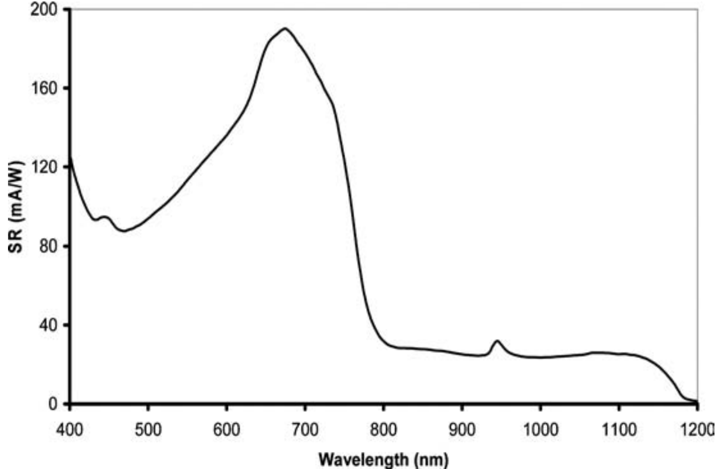

Figure 8.2 A typical responsivity-versus-wavelength curve measured for graded bandgap devices. Note the positive response in the IR region up to ~1,200 nm.

appropriate techniques are the current-voltage (I-V) measurements in the absence of UV and visible radiation to explore the PV activity of the device.

8.5.1 *I-V as a Function of Light Intensity*

In order to test the behaviour of these devices in diffused light, the device parameters were measured as a function of light intensity. Table 8.1 summarises the device parameters observed under different illumination conditions for a single device and two devices connected in series. It is an excellent feature of this device that the V_{oc} and FF values saturate to their highest values even at 1% of the one-sun intensity, of 1.2 mWcm^{-2}. In fact, this is almost completely dark, and the saturation of V_{oc} is a unique feature enabling the use of these devices in diffused light conditions. The production of V_{oc} = 980 mV and FF = 0.81 at 1% of the one-sun intensity indicates that there is a positive contribution from IR radiation towards the PV activity of this device, confirming the responsivity measurement results presented above. The two devices

Table 8.1 A summary of device parameters observed for 3 × 3 mm^2 solar cells, when measured individually and two cells connected in series, as a function of light intensity

Light Intensity	**One 3 × 3 mm^2 Cell**			**Two 3 × 3 mm^2 Cells in Series**		
Connected (mWcm^{-2})	**V_{oc}(mV)**	**FF**	**J_{sc}(mAcm^{-2})**	**V_{oc}(mV)**	**FF**	**J_{sc}(mAcm^{-2})**
1.2	980	0.81	0.10	1,960	0.81	0.12
10.5	1,080	0.83	1.20	2,160	0.83	1.26
53.0	1,140	0.85	6.19	2,270	0.85	6.49
100.0	1,150	0.85	12.12	2,310	0.85	12.14

connected in series further confirmed this observation and added up the two V_{oc} values as expected from a series connection.

8.5.2 *I-V Measurements Under Complete Darkness*

The above observation of the production of high values for V_{oc} and FF at the lowest light intensity guided the author's group to perform I-V characteristics under complete darkness and as a function of temperature. The devices were mounted inside a metal cryostat, eliminating background light completely, and the I-V characteristics were measured as a function of temperature. A typical set of linear-linear I-V curves observed under complete dark conditions are shown in Fig. 8.3.

The observation of J_{sc} and the production of V_{oc} values in the region of 650–850 mV under complete darkness confirms the PV activity created by thermal energy from the surroundings, and, hence, the existence of impurity PV activity in these devices. The variation of V_{oc} and J_{sc} as a function of temperature is as expected from a PV solar cell. V_{oc} decreases and J_{sc} increases as the temperature of the device is gradually increased.

In a separate I-V measurement system, diodes were measured under dark and illuminated conditions for further confirmation. Two such plots are shown in Fig. 8.4 in both linear-linear and log-linear forms. Again, the device exhibits ~1,175 mV and ~950 mV open circuit voltage under air-mass 1.5 (AM1.5) and in complete dark conditions, respectively, re-confirming the PV activity arising from IR radiation.

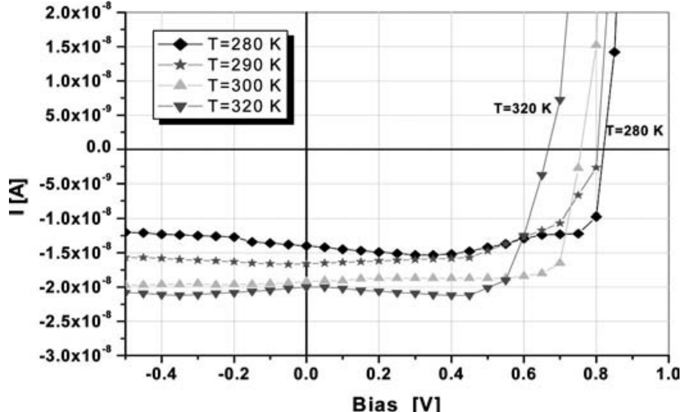

Figure 8.3 Linear-linear I-V curves measured for graded bandgap devices under complete darkness at different temperatures. See also Colour Insert.

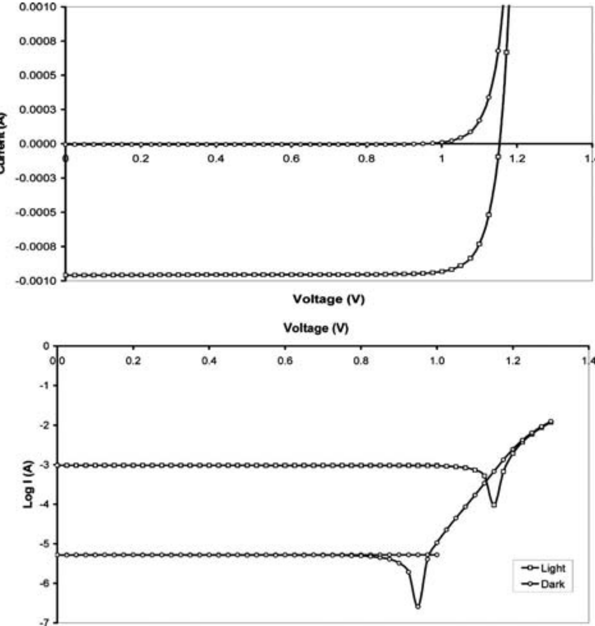

Figure 8.4 Linear-linear and log-linear I-V curves measured for graded bandgap devices under dark and AM1.5 illuminated conditions. Note the V_{oc} ≈950 mV produced in complete darkness and the V_{oc} ≈1,175 mV under illumination.

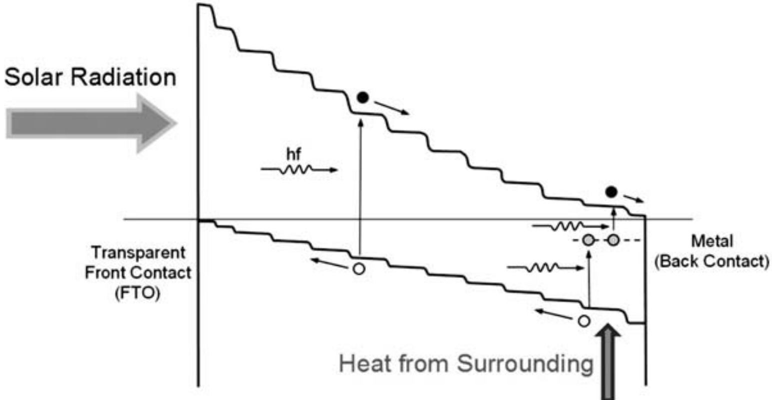

Figure 8.5 A schematic diagram showing the two energy inputs available to this device structure. When placed in complete darkness, the device still produces PV activity using the heat energy from the surroundings due to the impurity PV effect.

It is interesting to note the work by Bauhuis *et al.* [7] in 2007 on GaAs-based p-n type junctions. These devices have produced ∼40 mAcm^{-2} for J_{sc}, and therefore GaAs is capable of producing large short circuit current densities. As described in chapters 6, 7, and 8, when all the desired features as shown in Fig. 8.5 are achieved to improve optical absorption, incorporating the impurity PV effect and impact ionisation to enhance J_{sc}, this parameter could attain much larger values. Therefore, when fully optimised, this device has a huge potential to increase the conversion efficiency following the increase in J_{sc}.

8.6 Discussion

The above observations highlight the existence of two power inputs to these graded bandgap multi-layer solar cells, as shown in Fig. 8.5, (i) the normal solar radiation when illuminated and (ii) the surroundings of the solar cell acting as an infinite heat reservoir. The heat from the surroundings also creates charge carriers in the

Table 8.2 Experimentally observed defect levels in MOVPE $Al_xGa_{(1-x)}As$ layers [8, 9]

Al Content (x)	Activation Energy, E_a, (eV)	Approximate Concentration (cm^{-3})
0.05–0.11	0.41	10^{14}–10^{16}
0.15	0.50	10^{15}
0.20	0.55	10^{15}
(0.00–0.25)	(0.80–0.90)	The varying EL2 level according to the value of x

device, especially at the back end, and enhances the combined PV effect of the device. The production of charge carriers using IR photons depends on native defect levels, especially those occurring close to the growth substrate at the rear of the solar cell.

It is appropriate to look at the deep energy levels present in the MOVPE-grown $Al_xGa_{(1-x)}As$ layers. This material is the most researched semiconductor next to Si, and the the deep levels present are thoroughly studied and documented in the literature [8, 9]. Some of these are shown in Table 8.2; therefore, it is clear that there exists a ladder of deep levels in the bandgap. The concentration of these defects must be higher, closer to the GaAs substrate. These levels, therefore, must be helping to create charge carriers using multi-step generation (or the impurity PV effect), utilising IR radiation from surroundings.

Imagine the surrounding IR radiation promoting charge carriers to higher defect levels and accelerated photo-generated charge carriers promoting these electrons from defect levels to the conduction band. This will be another form of impact ionisation taking place in the device to create more photo-generated charge carriers in these devices. With this mechanism taking place when illuminated, each incoming photon is capable of producing more than one e-h pair. Therefore, this type of solar cells should show quantum efficiencies greater than unity when illuminated.

The detrimental recombination and generation (R&G) process also takes place in parallel, but the shape of this device allows the impurity PV effect to dominate and positively contribute to

the overall PV effect. Therefore, when fully optimised, this device has a huge potential to increase J_{sc} and, hence, the conversion efficiency.

8.7 Conclusions

The work presented in this chapter leads to several important conclusions.

The responsivity measurement as a function of wavelength is simple and experimentally confirms the existence of impurity PV effect in the graded bandgap multi-layer devices. These observations are re-confirmed by the production of high V_{oc} values together with other PV parameters in complete darkness. The theoretical expectation of the existence of the impurity PV effect is, therefore, experimentally confirmed for these new device structures.

The graded bandgap multi-layer solar cell structure has two power inputs, as shown in Fig. 8.5 — normal solar radiation and the surrounding heat energy. Heat energy creates charge carriers, and this process will enhance the overall PV effect of the device when illuminated. Therefore, when the doping concentrations are optimised to achieve fully depleted device, higher J_{sc} values and, hence, higher efficiencies are expected from this device design.

The current QE measurement systems miss out some important information, most probably due to the methods used for data collection, analysis, and/or presentations of the results. This may need re-examining and taking appropriate actions to improve this important PV characterisation technique.

8.8 Summary

A graded bandgap multi-layer solar cell device structure has been designed to effectively absorb UV, visible, and IR radiation and to incorporate impact ionisation and impurity PV effects within one

device. The design was experimentally tested with a well-researched material system, MOVPE-grown $Al_xGa_{(1-x)}As$. The highest-reported open circuit voltages of ~1,175 mV with the highest possible FF values (0.83–0.87) have been observed [1, 3] for the first two growths and fabrication. While the work is continuing to increase short circuit current density values, these devices were tested to explore the experimental evidence of the impurity PV effect, as expected from this design. Measurements of responsivity and PV activity in dark conditions have been carried out to investigate the impurity PV effect in these devices. Responsivity measurements indicate the current collection in the IR region, confirming the contribution from IR photons. The I-V measurements under dark conditions produced open circuit voltages exceeding 750 mV, confirming the contribution from the surrounding heat radiation. The new features of graded bandgap devices enable the impurity PV effect to dominate the detrimental recombination process and create useful charge carriers. This is possible because of the desired shape of the energy band edges present in the structure, which creates a high electric field within the device for the effective separation and collection of charge carriers.

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Chapter 9

Effects of Defects on Photovoltaic Solar Cell Characteristics

9.1 Introduction

The photovoltaic market currently consists mainly of Si, CdTe, CIGS, and III-V compound–based solar panels. There are some issues, especially on variations in performance measurements, stability, and lifetime. Some of these variations and behaviours, especially in thin-film solar cells, are not well understood at present. This chapter, therefore, addresses this subject. The experimental attempts made on this front, with possible explanations to the observed results and some solutions to reduce these undesirable behaviours, are presented in this chapter.

The experimental results are interpreted based on the observation of defect levels present in thin-film solar cells. The recently revealed new science [1, 2], as described in chapter 4, has shown the effect of several defect levels on CdTe-based solar cells. These ideas have also been extended to CIGS-based solar cells [3] in chapter 5. Developing the new ideas further, multi-layer graded bandgap solar cell structures have been proposed [4, 5], and these concepts have been experimentally tested using the well-researched GaAs/AlGaAs

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alloy system [5, 6]. These results have been presented and discussed in chapters 6, 7, and 8. GaAs/AlGaAs solar cells with high V_{oc} and fill factor (FF) values have been used to explore the measurement variations and stability issues commonly observed in thin-film solar cells. This chapter takes examples from CdTe, GaAs/AlGaAs, and CIGS solar cells in order to highlight these variations during current-voltage (I-V) measurements.

9.2 Variations of I-V Characteristics of Metal/n-CdTe Interfaces

Before discussing instabilities of fully fabricated solar cells, it is worth summarising the work reported in 2005 on metal/n-CdTe single interfaces in the presence of a set of defect levels [7]. Typical forward and reverse I-V characteristics of metal/n-CdTe diodes are shown by curve-1 in Fig. 9.1. These diodes exhibited good rectification properties, and the ideality factors (n) varied in the range 1.10–1.95. The potential barrier height (ϕ_b) estimated using the standard method [8] was in the range of 0.96 ± 0.04 eV. However, the details of I-V curves varied from measurement to measurement and also according to the immediate history of the diode. For example, the value of n varied slightly based on the direction of data collection (whether the I-V curve was measured from reverse to forward bias or vice versa) and the conditions of storage of the diode prior to measurements (whether the diode was stored in the dark or in room illumination conditions). To study these variations in detail, a selected diode was forward biased with a voltage value of 1.0 V for a period of 1 hour and the I-V curve was measured immediately after the removal of the bias voltage. Many diodes showed very different I-V curves with reduced barrier heights, and a typical I-V curve is shown by curve-2 in Fig. 9.1. These diodes also exhibited values of n in the range 1.10–2.00, enabling the accurate estimation of barrier heights. The estimated barrier heights were much less than the original value, and typical barriers were in the range 0.70–0.77 eV. After recording the I-V characteristics, the same diode was exposed to a reverse bias of 1.0 V for a longer period (over 10 hours). During the application of a bias voltage, the diode was kept under

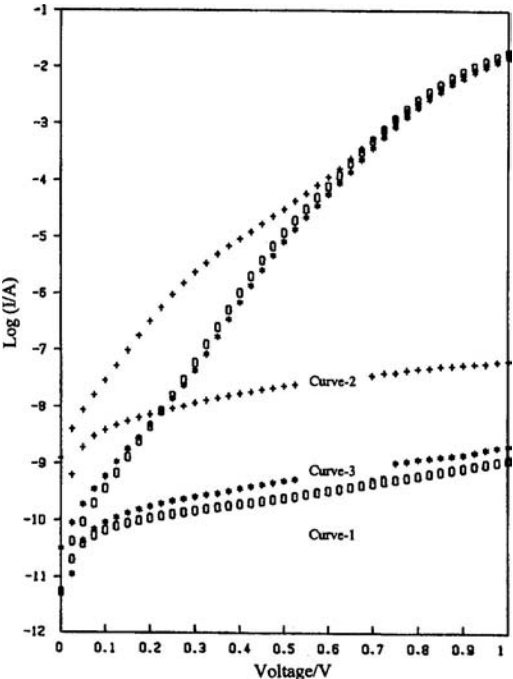

Figure 9.1 Typical changes in I-V characteristics of Au-Sb/n-CdTe contacts with applied electrical stress. Curve-1: The I-V curve of an as-made diode; Curve-2: The deteriorated I-V curve of the same diode after application of 1.0 V forward bias for 1 hour in dark conditions; Curve-3: The improved I-V curve after reversal to the original position when 1.0 V reverse bias was applied for 10 hours under dark conditions.

dark condition to avoid the effect of light on the diode. In many cases, it was possible to revert to the original I-V curve, as shown by curve-3 in Fig. 9.1. This reversal of I-V would vary from diode to diode, and some needed only a few hours but others needed a longer period of reverse-bias application. These results were observed in the mid-1980s, but the behaviour could not be explained fully during that time although the consensus was that this is due to effects of slow traps.

With the improved understanding of metal/n-CdTe interfaces as described in chapter four, these results can now be fully explained using defect levels present at this interface. The energy band

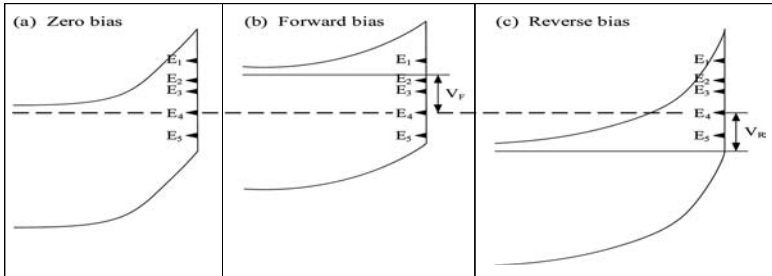

Figure 9.2 The experimentally observed five Fermi-level pinning positions at metal/n-CdTe interfaces. (a) At zero bias, the Fermi level is pinned at level E_4; (b) the application of the forward bias, V_F, across the diode starts to fill E_2–E_4 levels with electrons, and when V_F is removed, the Fermi-level pinning may take place at E_2, E_3, or E_4; (c) the application of reverse bias starts to de-trap electrons from E_1–E_5 and when released, the Fermi-level pinning may take place at a different energy level at E_5 or E_4.

diagrams of these interfaces with five possible Fermi-level pinning positions are shown in Fig. 9.2. The three diagrams represent the zero-bias, the forward-bias, and the reverse-bias conditions, respectively. Forward-bias conditions allow trap levels to fill with electrons, and the reverse bias allows these levels to empty due to their relative positions with respect to the Fermi level. Also, the forward-bias condition is equivalent to the open circuit situation of a solar cell under illumination or the solar panel used during the daytime. During night-time, a solar cell has the zero-bias condition and, hence, the defects situated above the Fermi level will de-trap during dark conditions. This work has demonstrated that the forward bias or illumination of active junctions with existing defect structures could produce lower potential barriers or lower V_{oc} values and, hence, lower conversion efficiencies. During the forward-bias condition, all trap levels will be filled and, therefore, the Fermi level will pin at a lower level upon removal of the applied stress (electrical or light). These conditions can be reversed by applying reverse-bias voltages or leaving the devices under dark conditions for several hours.

Similar situations may arise when I-V measurements are repeated within a period of a few minutes. For example, during an I-V curve measurement cycle, say between -1.0 and $+1.0$ V, the

Fermi level moves at the interface from forward bias to reverse bias, or vice versa. In the presence of a set of deep traps at the interface, the Fermi level crosses these levels and allows them to trap or de-trap electrons according to the location of the defect level with respect to the Fermi level. This will, in turn, allow the Fermi level to switch between defect levels and, hence, affect the ϕ_b and the properties of I-V characteristics measured.

9.3 Effects on the Performance of CdS/CdTe Solar Cells

Similar variations have also been observed in fully fabricated CdTe-based solar cells. Figure 9.3 shows the proposed energy band diagram of the glass/TCO/CdS/CdTe/metal thin-film solar cell according to the new model [1, 2]. For this model the CdTe layer remains n-type with the existence of an n-n-graded hetero-junction at the CdS/CdTe interface together with a large Schottky barrier at the back metal contact. The defect levels E_1–E_5 are related to native defects, and their concentrations can be changed by material growth conditions, post-growth modifications such as chemical treatments,

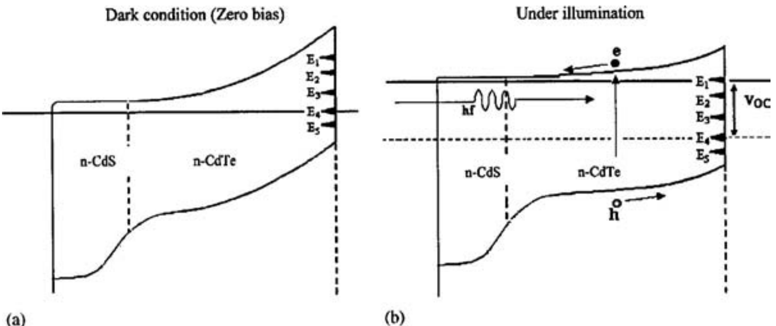

Figure 9.3 (a) The energy band diagram of the CdS/CdTe solar cell according to the new model, showing a combination of a graded n-n hetero-junction and a large Schottky barrier at the back metal contact. (b) Under illumination, the device produces an open circuit voltage of V_{oc}, and this is identical to application of a forward bias of $V = V_{oc}$. The pinning position could, therefore, move upward, resulting in poor parameters for the solar cell during the second measurement or after illumination.

heat treatments, and chemical etching. When the Fermi level is pinned at the E_5 level, it produces the largest Schottky barrier at the metal/CdTe interface, creating an excellent band bending or the highest internal electric field across the device. This will produce a good solar cell due to the existence of a strong internal electric field for charge carrier separation and collection. If the conditions are favourable to pin the Fermi level at E_1, the band bending will be at a minimum and, therefore, the internal electric field will be weak. Consequently, this will form a very poor solar cell. Since there are five possible Fermi-level pinning positions, the resultant solar cells will vary from laboratory to laboratory and, sometimes, from batch to batch within the same laboratory. This effect can show severe problems in reproducibility and yield during a solar cell production process. In such a situation, when the I-V curves are measured, for example between $+1.0$ and -1.0 V, the Fermi level will be swept across the five defect levels. For example, in the forward-bias sweep, E_1–E_5 levels will be below the Fermi level for a certain period of the measurement time and, therefore, the defects will trap electrons — Fig. 9.3(b). In the reverse-bias sweep, all the defect levels are above the Fermi level and, therefore, the defects will de-trap electrons during this period. The observations indicate that these traps are very slow to respond but sensitive to electrical, thermal, and lighting stresses applied to the device. Figure 9.3(b) shows the open circuit voltage developed when the device is illuminated, and this is identical to the forward biasing of the device under dark conditions by $V = V_{oc}$. Therefore, the I-V characteristics of the devices can vary even after exposure to light, depending on the concentration of defects at the interface. If the trapping during illumination is considerable, the Fermi-level pinning position can move upwards, showing a lower V_{oc} when measured for the second time.

The effects of multi-defect levels at the metal/CdTe interface of CdS/CdTe solar cells are demonstrated by the data presented in Table 9.1.

When solar cell-1 was measured for the first time, the V_{oc} was 610 mV and the J_{sc} was 32 mAcm^{-2}. When the I-V measurements were repeated consecutively at intervals of a few minutes, the V_{oc} reduced drastically and finally settled at 280 mV, indicating the shift of Fermi-level pinning position in the direction E_5 to E_1, reducing

Table 9.1 The variation of CdS/CdTe solar cell parameters for consecutive measurements under identical conditions

	Solar Cell-1		Solar Cell-2	
Measurement	V_{oc} (mV)	J_{sc} (mAcm^{-2})	V_{oc} (mV)	J_{sc} (mAcm^{-2})
1	610	32	650	29
2	400	32	640	29
3	280	30	655	29
4	280	29	650	29

the value of the ϕ_b, and hence the V_{oc}. However, the current density remained almost constant within experimental error, due to the presence of adequate band bending for the collection of photo-generated charge carriers. In comparison, solar cell-2, made on the same sample, showed stable V_{oc} and J_{sc} values for different measurements, indicating the pinning of the Fermi level at a fixed level, and other defects had low influence, presumably due to their low concentrations. For a practical solar cell, this is desirable, and solar cell-1 has very high concentrations of different defects and, therefore, shows undesirable changes of V_{oc}. Since the exposure of the solar cell to sunlight is equivalent to forward biasing, and keeping the solar cell in the dark is equivalent to zero biasing of a diode, solar cell deterioration during daytime and the recovery during night-time can be explained in terms of trapping and de-trapping of electrons by slow defects. This is indeed a common feature observed during present-day solar panel monitoring processes.

9.4 Variations in GaAs/AlGaAs Solar Cells

Having observed variations in the I-V characteristics of CdTe-based single interfaces and fully fabricated solar cells, this idea can be tested using GaAs-based solar cells. The devices described in chapters 6, 7, and 8 have been used to explore these behaviours further.

9.4.1 *Device Structures Used*

The energy band diagram shown in Fig. 9.4(a) has been selected as the suitable design for the production of multi-layer graded

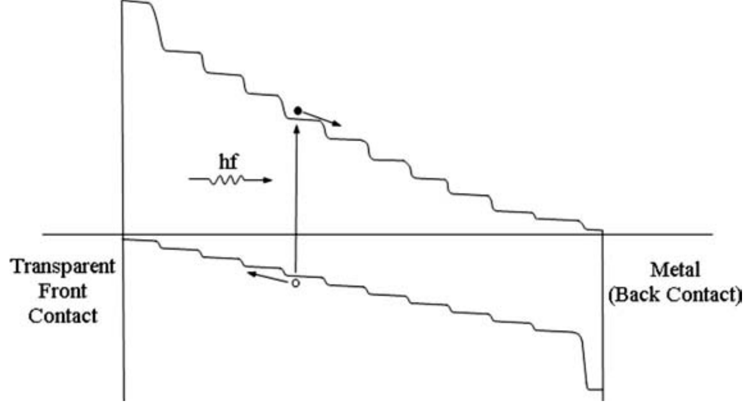

Figure 9.4a An idealised design of the multi-layer graded bandgap solar cell structure.

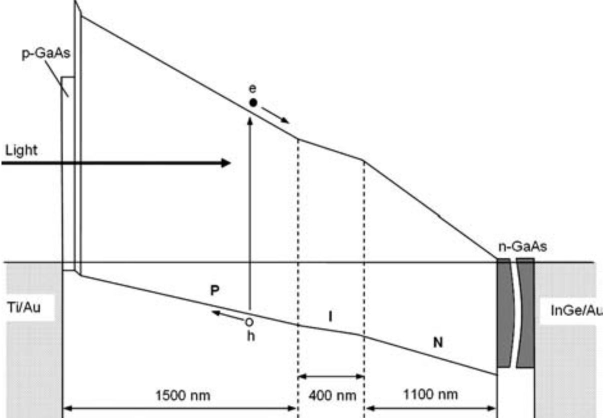

Figure 9.4b The closest sketch of the energy band diagram expected for the AlGaAs/GaAs solar cell after growth using the metalorganic chemical vapour deposition (MOVPE) method and studied in this work.

bandgap solar cell structures [4]. The closest sketch of the energy band diagram of this device structure after fabrication is given in Fig. 9.4(b), and the total thickness of the solar cell structure is about 3 μm [5, 6]. The lab-scale devices were processed as described in the 2006 publication [5] and in chapters 6 and 7. The device areas of the

two types of solar cells used were 0.002 cm^2 (0.5 mm diameter) and 0.090 cm^2 (3 × 3 mm^2). The larger devices also had 120 nm thick MgF_2 anti-reflection coating.

9.4.2 *Instability of I-V Characteristics*

A typical set of I-V characteristics for 3 × 3 mm^2 solar cells is shown in Fig. 9.5, and some measured parameters are summarised in Table 9.2. The FF values of these devices are above 0.80, and the highest measured V_{oc} value is 1,150 mV. As shown in Fig. 9.5, the I-V characteristics show excellent properties and these diodes were selected for studying the effects of defects in solar cells when tested after stressing from their equilibrium state.

9.4.3 *Application of Electrical Stresses to the Device*

The devices selected were first measured for evaluation of their solar cell parameters (V_{oc}, J_{sc}, and FF), and then electrical stresses were applied while the devices were kept at room temperature and in dark conditions [9]. For example, the diodes were forward biased with a voltage of ~0.9 V for several hours and I-V curves were

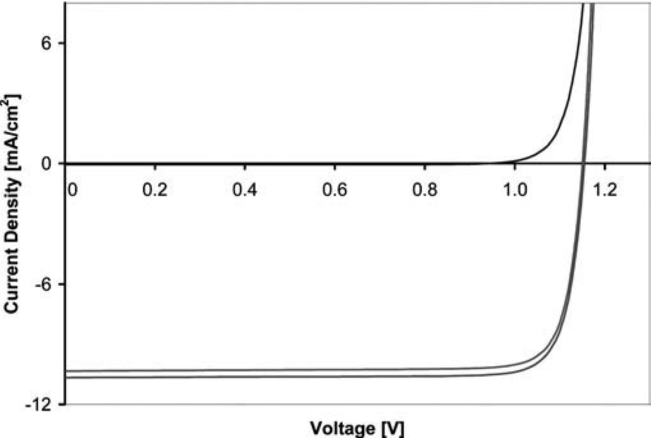

Figure 9.5 I-V characteristics measured for two 3 × 3 mm^2 solar cells under air-mass 1.5 (AM1.5) conditions. Only one dark I-V curve is shown for clarity, and the other curve is very similar. See also Colour Insert.

Table 9.2 Typical solar cell parameters measured under AM1.5 conditions for 0.002 cm^2 and 0.090 cm^2 solar cells

Device		V_{oc}(mV)	J_{sc} (mAcm^{-2})	FF	η (%)	R_s(Ω/cm^2)	R_p(Ω/cm^2)
0.002 cm^2	1	1,110	12.6	0.83	11.6	—	—
solar cells	2	1,081	12.3	0.82	11.0	2.3	4,200
	3	1,077	12.3	0.82	10.8	2.9	3,000
0.090 cm^2	1	1,148	11.9	0.86	11.7	2.5	10,400
solar cells	2	1,141	11.4	0.86	11.2	4.0	5,100
	3	1,150	13.1	0.85	12.7	3.8	—

measured immediately after the removal of the bias voltage. The same diodes were then exposed to reverse-bias conditions with a voltage of ~0.8 V for several hours and I-V curves were immediately recorded. Drastic changes in I-V characteristics have been observed, distorting the high-quality solar cell characteristics presented in Fig. 9.5. Typical results are summarised in Table 9.3 and shown in Figs. 9.6 to 9.9.

During subsequent I-V measurements after applying electrical stresses to device structures, measured parameters showed drastic changes, as shown in Table 9.3. All parameters fluctuate in wide ranges. The I-V curves showed peculiar kinks, as shown in Fig. 9.6; sudden discontinuities, as shown in Fig. 9.7(a); and deformed characteristics, as shown in Fig. 9.7(b). Figure 9.8 graphically

Table 9.3 A summary of solar cell parameters as a function of the applied external electrical stress

	Stresses Applied (V)	V_{oc}(mV)	FF (%)	I_{sc} (mA)	J_{sc} (mAcm^{-2})
1.	First measurement	1,093	84	0.036	18.0
2.	Forward bias with 1.0 V for 2 hrs	930	73	0.037	18.3
3.	Forward bias with 1.0 V for 3 hrs	855	77	0.023	11.4
4.	Reverse bias with 0.7 V for 17 hrs	855	74	0.032	16.1
5.	Reverse bias with 0.8 V for 3 hrs	888	77	0.021	10.7
6.	Reverse bias with 0.8 V for 19 hrs	1,038	83	0.012	6.0
7.	Reverse bias with 0.8 V for 3 hrs	963	54	0.045	22.5
8.	Reverse bias with 0.8 V for 19 hrs	1,081	81	0.028	14.1
9.	Forward bias with 0.9 V for 66 hrs	1,050	82	0.016	7.8
10.	Forward bias with 0.9 V for 28 hrs	625	62	0.024	12.0
11.	Forward bias with 0.9 V for 25 hrs	1,025	80	0.009	4.6

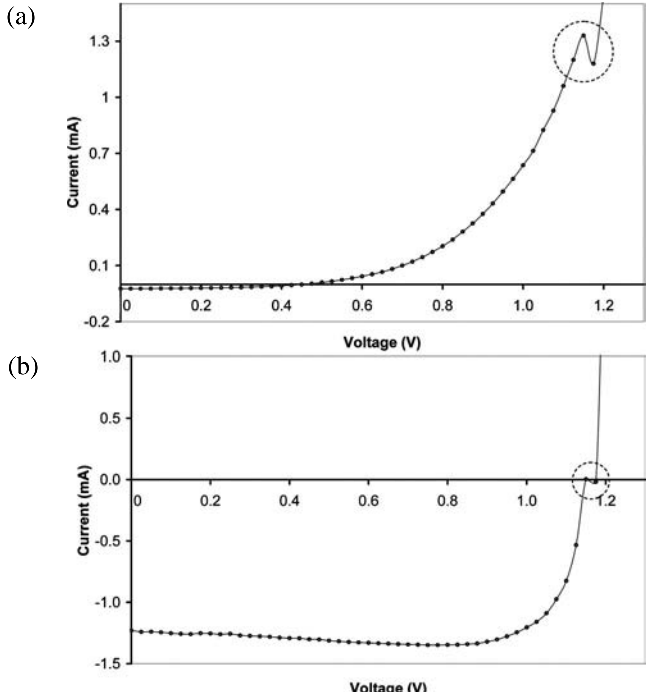

Figure 9.6 Kinks observed during I-V measurements of 0.5 mm diameter solar cells after the application of various electrical stresses to the diode. These kinks appear randomly at different places of the I-V curve.

summarises the variation of V_{oc} and FF values observed after various conditions are applied to two 0.5 mm diameter solar cells. Figure 9.9 summarises similar results obtained for two 3×3 mm^2 solar cells.

9.4.4 *Discussion and Possible Explanations*

It is now appropriate to discuss the defect levels present at the two interfaces of the device under investigation. Defects on both GaAs [10, 11] and AlGaAs [12, 13] layers have been thoroughly studied and reported in the past, and the main electron traps are shown in Fig. 9.10. As described before, these defect levels can drastically affect the I-V characteristics of the device. For example, when the Fermi level sweeps along the metal/AlGaAs interface during I-V

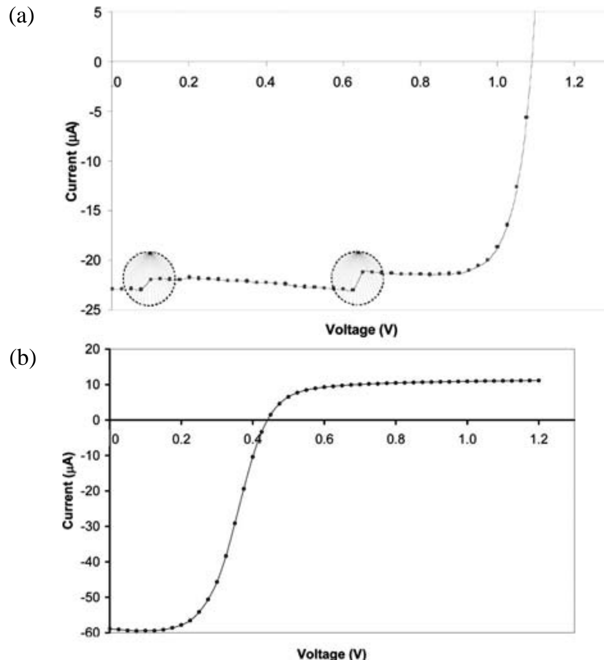

Figure 9.7 Sudden discontinuities and completely distorted I-V curves observed during measurements after the application of external electrical stresses to diodes and then removed.

measurement cycle or during the application of electrical stresses, the Fermi level could switch onto different positions, producing diodes of different barrier heights. These device structures with numerous defect levels at their interfaces, therefore, could produce different I-V characteristics, depending on the immediate history of the device. Some of the possible different I-V curves are shown with dotted lines in Fig. 9.11 with different potential barriers. During the switch-over from one I-V curve to another, peculiar kinks and sudden discontinuities could occur, as shown in the diagrams. These kinks and discontinuities could appear at different positions depending on the defect structures, defect densities, and their electron occupation.

Since this diode has two interfaces with complex defect structures, the Fermi level crosses defect levels on both interfaces.

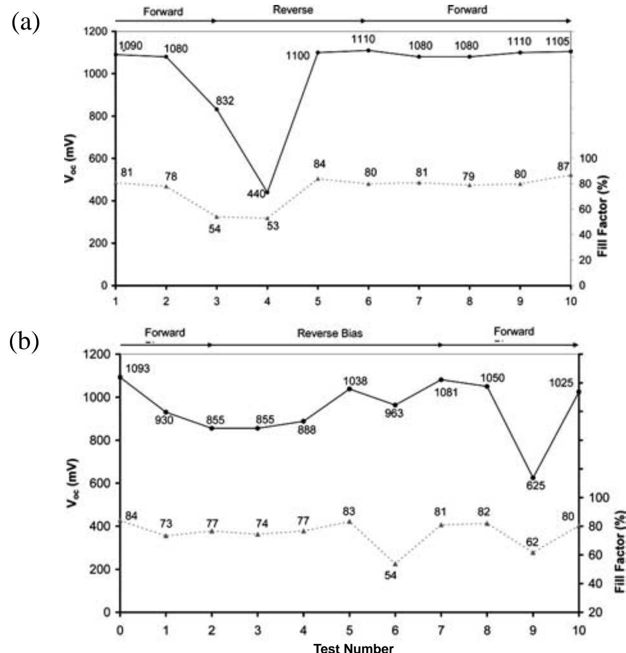

Figure 9.8 The variation of V_{oc} and FF as a function of applied forward- and reverse-bias electrical stresses on two 0.5 mm diameter solar cells.

When the right conditions have been established, it is possible to shift the Fermi-level position to form a distorted energy band diagram, as shown in Fig. 9.12. For example, the application of reverse-bias stress to this device structure and removal could easily trigger the Fermi-level shift to a lower position at the AlGaAs/GaAs interface. When this happens, there are two diodes in the device structure connected opposite to each other and the typical I-V curve represented by Fig. 9.7(b) will be the final result. This situation corresponds to test number 4 of Fig. 9.8(a); note the drastic reduction of solar cell parameters ($V_{oc} \approx 440$ mV and FF ≈ 0.53) due to the weakened main diode. At large forward-bias voltages, the main diode reaches flat-band conditions and the reverse-bias properties of the smaller diode at AlGaAs/GaAs interface dominate I-V characteristics, showing its saturation current in the first quadrant.

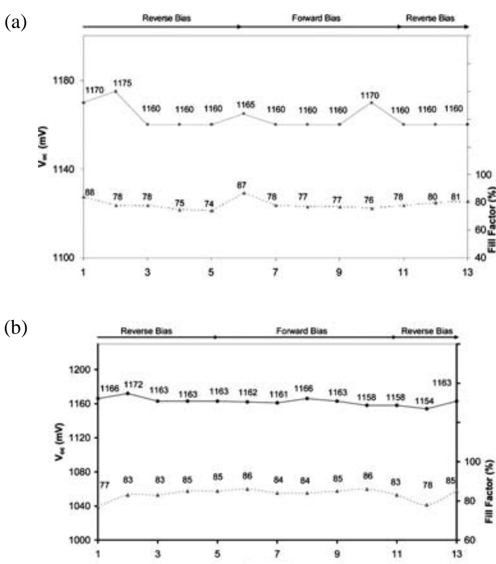

Figure 9.9 The variation of V_{oc} and FF as a function of applied forward- and reverse-bias electrical stresses on two 3×3 mm^2 solar cells.

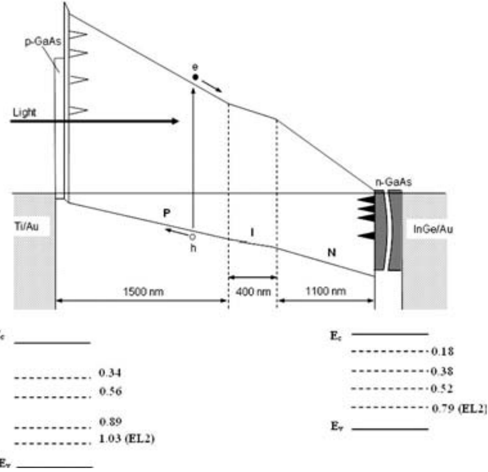

Figure 9.10 A sketch of the energy band diagram of the AlGaAs/GaAs solar cell together with well-established defect levels present in AlGaAs and GaAs materials near metal contacts.

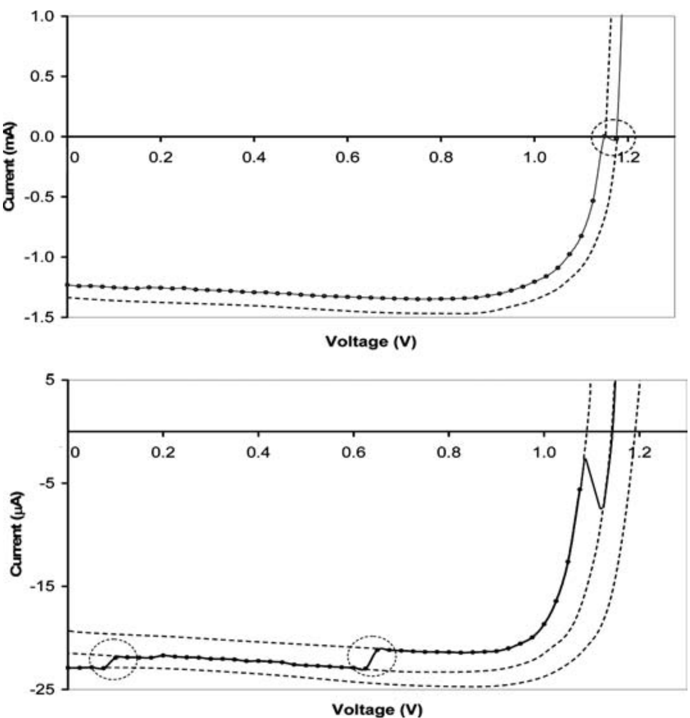

Figure 9.11 Sudden discontinuities and kinks observed in I-V curves, showing the Fermi-level changes from one position to another, producing different I-V characteristics corresponding to different ϕ_b values.

Figure 9.8(a) represents a clear example of the reduction of V_{oc} as a result of forward biasing and the reversal to the original value after reverse biasing. With further forward biasing, this particular diode (0.5 mm diameter) shows stable behaviour after this first variation, indicating a permanent change such as a removal (or passivation) of temporary defects existing at the interface. These types of temporary defects may arise due to trapped charges at the interface. On the other hand, the diode shown by Fig. 9.8(b) shows reversible behaviour. A forward bias reduces V_{oc}, and a reverse bias restores the value to original figures, with V_{oc} again reducing after further forward biasing. This behaviour seems reversible for this diode, indicating the presence of a set of permanent defect structures at the interface.

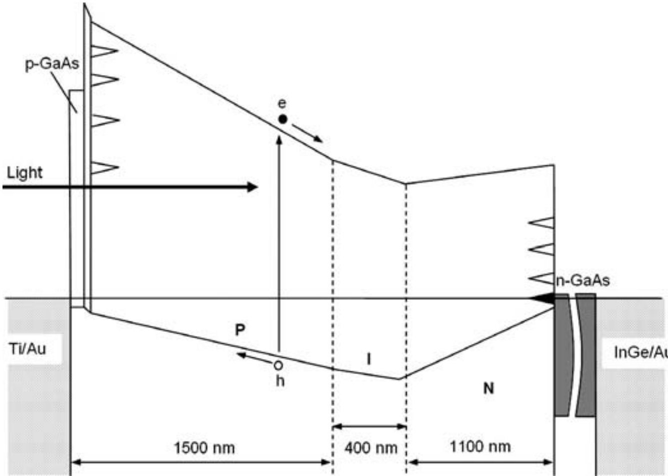

Figure 9.12 The deformation of the energy band diagram during reverse biasing, followed by the release of the electrical stress. A second diode is formed at the AlGaAs/GaAs interface due to a Fermi-level shift to a lower energy level.

The results shown by Fig. 9.9 for 3×3 mm^2 solar cells seem to be very stable, showing the most desirable qualities needed for a practical solar cell. These 3×3 mm^2 solar cells have a 120 nm thick MgF_2 anti-reflection coating when compared to 0.5 mm diameter devices. Low concentrations of unwanted defects at interfaces during processing may have improved the device parameters.

It should be noted that the filling and emptying of defect levels are also influenced by changes in temperature and light intensity in addition to the electrical stresses externally applied to the device. Therefore, the results may vary according to the dominant effect at a particular situation. The deterioration of V_{oc} during daytime or the light soaking (equivalent to the forward-biasing effect) and recovery effect during night-time (equivalent to a zero-bias situation) observed for solar cells can be explained in terms of defects in the semiconductors or at the interfaces. The removal (or passivation) of unwanted defects in solar cells will allow the production of high-efficiency solar cells and reduce these undesirable instability effects.

9.5 Variations in CIGS Solar Cells

Comprehensive work on electrodeposited CIGS-based solar cells also shows different shapes of I-V curves for different batches of devices, similar to those of CdTe-based solar cells. These different types of I-V curves are sketched in Fig. 9.13, and three major groups are labelled as curves A, B, and C. Curve A represents the desired solar cell characteristics, observed when the defect concentrations are low or inactive in the device structure. The other extreme is shown by curve C, where the photo-generated charge carriers are removed drastically by defects through the recombination process and, hence, the current in the external circuit is low and the FF reduces drastically. The amount of recombination varies according to the defect levels present, their location and concentrations, and the Fermi-level position at the interface. Depending on the circumstances, any shape between A and C could be measured. The special situation shown by curve B is also observed, but this linear behaviour is only one of the many possibilities and not due to higher series resistance of the device structure. Similar results have been reported by Platzer-Björkman *et al.* [14] for solar cells based on CIGS grown by the vacuum evaporation method.

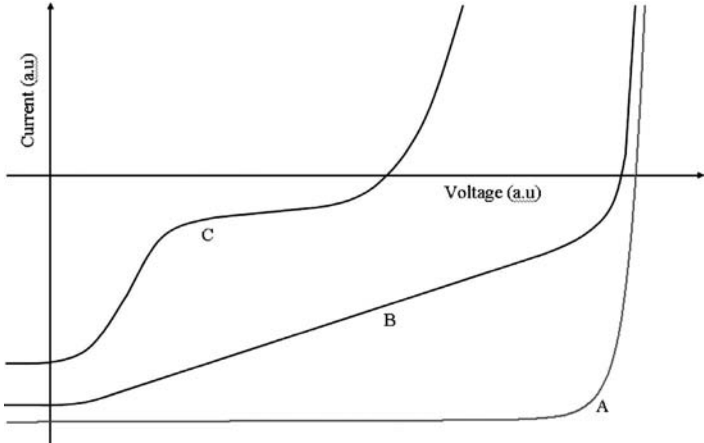

Figure 9.13 Different shapes of I-V curves observed for solar cells based on electrodeposited CdTe and CIGS materials.

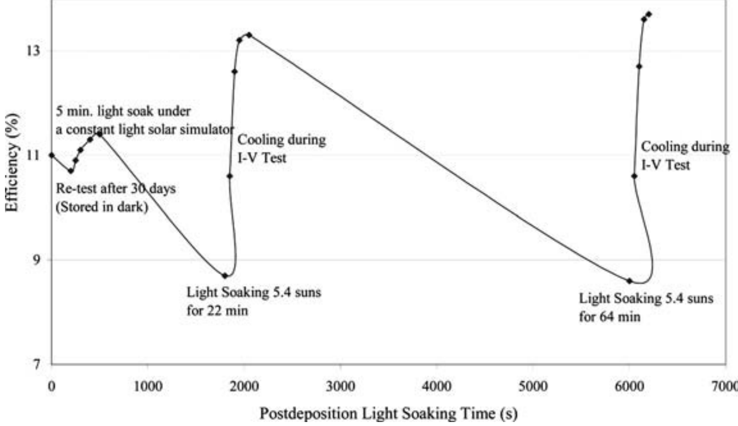

Figure 9.14 The instability of Showa-Shell CIGS solar panels, reported by Kushiya *et al.* in 2003, during stability studies of solar panels (re-drawn from ref. [16].

The unstable behaviour of Showa-Shell CIGS solar panels, as reported by Kushiya *et al.*, is another good example [15]. Although these Showa-Shell CIGS panels produce large-area modules with high efficiencies [16], major features of instabilities are reported in 2003, as shown in Fig. 9.14. It is clear that the light soaking of solar panels reduces the efficiency from ~11.5% to ~8.5%. However, cooling during the I-V test increases the efficiency back to their maximum values of ~13.3%. This is mainly due to the quenching of R&G activities by freezing defect activities at lower temperatures. The presence of a set of defect levels in the Showa-Shell CIGS material has been experimentally observed and recently reported [7]. The identification of the origin of these defect levels and their removal (or passivation) will eliminate these undesirable instability issues and produce stable and high-efficiency solar panels.

The usually observed trade-off between the two parameters V_{oc} and J_{sc} can also be understood in terms of defect structures present in solar cells. The results reported in 2005 by Contreras *et al.* [17] together with the general observation of improved V_{oc} values with corresponding reduced J_{sc} could be explained as follows. Whatever, the device structure used, there exists an active PV junction with a set of defect levels. As an example, consider the simplest situation

shown by Fig. 9.2. The following explanations are equally applicable for any other junctions based on p-type or n-type semiconductors. Consider a solar cell based on a metal/semiconductor (MS) interface with five defect levels present, as shown in Fig. 9.2. The R&G is highest due to the E_3 level, situated in the middle of the bandgap. In the case of Fermi-level pinning at E_4 or E_5 levels, high V_{oc} values are obtained but the R&G is extremely high due to actions of the empty E_3 level. The ultimate result is the observation of a high V_{oc} with a low J_{sc} value. On the other hand, if the Fermi level is pinned just above E_3, the results will be a low V_{oc} value but a drastic reduction of R&G activities due to a filled or saturated E_3 level. When there is sufficient band bending to collect photo-generated charge carriers due to Fermi-level pinning above the E_3 level, a low V_{oc} and a high J_{sc} will be the final result.

A large body of experimental evidence published on amorphous and polycrystalline Si solar cells also shows degradation due to light soaking [18, 19]. There are also numerous reports in the literature on solar panel degradation during daytime and recovery during night-time. These behaviours are identical to properties explained in this chapter on solar cells based on CdTe, AlGaAs, and CIGS. This commonality in all thin-film solar cells highlights the importance of the effects of defects in semiconductors on the performance and reliability of solar panels.

It is becoming clear that all CdTe [1, 2], CIGS [7], AlGaAs [10–13], and thin-film Si [18, 19] solar cells have complex defect structures at their active interfaces. The identification and removal (or passivation) of defects is, therefore, becoming crucial in improving the reproducibility, performance, stability, yield, and lifetime of PV solar cells. This improved understanding of solar cell structures could lead to the achievement of stable, low-cost, and highly efficient solar cells in the future. This impact could be seen in all thin-film PV solar cells based on Si, III-V compounds, CdTe, and CIGS, which are currently undergoing intense research and development process.

9.6 Summary

The results presented and discussed in this chapter lead to the following conclusions.

There are drastic effects of defects on PV solar cell reproducibility, yield, device performance, and stability. The reproducibility of devices can be severely affected by the presence of several defect levels, leading to pinning at different positions and, hence, producing varying efficiencies. The nature of measured I-V characteristics can be affected by external forces such as applied electrical stresses, light soaking, heating, or cooling. Because of the effects of a series of defects, the shape of I-V curves can be changed after repeated measurements due to the direction of data collection. It has been found that peculiar kinks, sudden jumps, and various deformations could occur in I-V curves when the Fermi-level position moves at the device interface. These changes occur when there is a group of defect levels and the Fermi level is forced to move across these levels. When a series of defects is present in the active junction area, improvement of V_{oc} is observed with a corresponding reduction of J_{sc} values and vice versa. The FF and current density values are drastically affected by the presence of active R&G centres. The above variations are observed for devices with defects of considerable concentration. The undesirable behaviours of solar cells based on inorganic materials are mainly due to defects in the bulk materials, interfaces, or the combination of both. In order to produce high-efficiency, stable, and long-life solar cells, defect identification, keeping the benign defects, and the removal (or passivation) of detrimental defects are essential. The establishment of these conditions for solar cells based on different materials and structures will lead to considerable improvement of PV solar cell performance in the future.

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Chapter 10

A Future Dominated by Solar Energy

10.1 Introduction

Fossil fuels provided the backbone of the industrial revolution, contributing enormously to the development of modern society, but were of benefit only to some, not all, of the world's population and also polluted the environment and increased the relative proportion of greenhouse gases in the atmosphere. Population growth, coupled with climate change (contributed by the burning of fossil fuels), is presenting the human world with perhaps its most severe problem and challenge in living history.

Fossil fuel is derived from organically generated carbon, that is, former living organisms. As such, it is a finite resource — not renewable. For the past 200 years, these natural resources have been used at an increasing rate, with no thought for sustainability and future generations. Easily accessible fossil fuels are being used, and extraction costs are rising. Therefore, the way forward is to use fossil fuels in an efficient and more controlled manner while introducing renewable energy sources, including biomass, hydro-electricity, photovoltaics, solar thermal, wind, tidal and wave. Of the renewable energy sources, solar power has the highest potential to develop society and reduce poverty in the future. This chapter

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Figure 10.1 The use of solar energy in low-power and DC applications for convenience. See also Colour Insert.

presents various solar energy applications that can lead to a safe and peaceful world.

10.2 Early Applications with Low Power Requirements

With the production of commercial solar cells in the 1950s, a large expansion was seen in low-power applications, such as solar-powered calculators and wrist watches. The power requirements were less than 1.0 W, but the convenience created by eliminating regular battery changes attracted these applications. The car parking meters introduced in the 1990s are examples of an application that rapidly expanded because there was no need to dig for cables during installation. Apart from the low power requirements, there are other environmental benefits that make these applications attractive to the modern society. In the future, these low-power and direct current (DC) applications will continue to grow and solar cells based on organic materials will have a place in these low-power applications (Fig. 10.1).

10.3 Early Applications with Moderate Power Requirements

One of the first commercial uses of solar cells was in the late 1950s as a power source for space satellites. Solar panels were then used

Figure 10.2 The use of solar energy in remote locations such as health centres.

to power remote communication and health centres built away from national grids. Solar energy coupled with wind energy became a popular combination for various applications in other strategic applications in remote areas (Fig. 10.2).

10.4 Applications in Solar Home Systems (~50 W Range)

One-third of the world's population (over 2 billion people in the year 2000) was not connected to power grids; therefore, the domestic lighting arrangements of these people were mainly based on kerosene oil. The PV industry has developed stand-alone solar home systems powered by a ~50 W solar panel. These systems provide for basic needs like lighting and power for the radio and television and help to improve health, education, and the standard of living for the poorest section of the population. The television is the main attraction for the rapid market penetration of this system. These applications started with black-and-white televisions but soon improved for use in colour televisions. In Sri Lanka, for example, about 20% of the population has no electricity from the grid and these applications have been growing rapidly over the past two decades (Fig. 10.3). In the early 1990s, one or two local companies were struggling to install these systems, without making profits, but today, over a dozen such companies install these systems round the country, making a profitable business. There are about 150,000 solar home systems installed in the country at present, and this is equivalent to ~7.5 MW power generation,

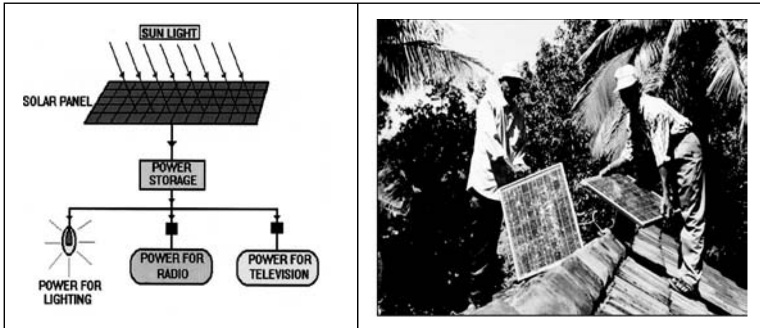

Figure 10.3 The main features of a basic solar home system, and two technicians installing a system on a rural village home in Sri Lanka.

eliminating power cables around. The local solar energy companies are currently creating new jobs for young people and install about 2,000 solar home systems per month. This rate seems to be very impressive, but Sri Lanka has about 1 million rural homes that cannot be easily served by the national grid, and it would take about 40 years to complete village electrification using solar power at the current rate. To achieve full village electrification in five years, an eight-fold expansion of the solar power sector is required. There is an urgent need for both the expansion of existing companies and an increase in the number of solar energy companies within Sri Lanka. Concentrating on a 'large number of small systems' will have a huge impact at this stage for the needy people in developing countries.

Businesses based on solar energy are now rapidly gaining popularity in many developing countries. The beauty of the development of this industry is that when the national grid develops and expands, the households can use these solar panels for other small applications.

In current solar home systems, low-power fluorescent lamps are used with DC electricity. Over the coming years, domestic lighting is likely to be replaced by low-power light-emitting diodes (LEDs), also operating on DC electricity, consuming low electric power.

With the introduction of LED lamps for domestic lighting, the solar home systems now popular in rural areas in developing

countries will have applications in developed countries also. Such LED lamps can be powered by one or two solar panels fixed on roofs in developed regions, creating a large demand for solar energy application companies. In addition to solar home systems, there are numerous applications in the 50 W power range; street lighting, solar lanterns, solar-powered telephone booths, and traffic lights are only some.

10.5 Applications in Drip Irrigation Systems (∼100 W Range)

Being an agricultural country with about 80% of the population living in villages, Sri Lanka is likely to experience rapid development in food production with small drip irrigation systems powered by single solar panels of ∼100 W each (Fig. 10.4). This requires only a 1 m^2 solar panel with a 10% conversion efficiency. At present, Sri Lanka has the largest solar-powered drip irrigation programme in the world, introduced by the Ministry of Agriculture. Five thousand systems have been distributed in the dry zone, and some of them are used very effectively to produce crops, increasing additional income for village families. More systems should be installed in every part of Sri Lanka among village communities in order to reduce poverty in these communities and enhance the most-needed food production. Although the additional power produced by these 5,000 systems at the place of energy requirement is only 0.5 MW, the impact of these through wealth creation, social development, and reduction of poverty is substantial.

Many parts of the world are slowly becoming deserts, and the rate is alarming. Drip irrigation using the plentiful sunshine available will create the food we require and slow down the detrimental desertification. Introduction of organised tree-planting projects will convert sandy lands to a green carpet, converting arid areas to pleasant oases. With the expected population of 9–10 billion people by the middle of the 21st century, habitable lands should be preserved and more food should be produced. Solar technology will help to establish both if these applications are rapidly introduced in society.

Figure 10.4 A solar-powered drip irrigation system — an excellent method to enhance food production, stop desertification, and preserve habitable lands for the growing world population.

10.6 Applications in Powering Computers (500–1,000 W Range)

There are numerous applications in this power range. Figure 10.5 shows one example — the first solar-powered computer system in Sri Lanka. An 800 W system has been installed at Hunugallewa School in Sri Lanka to power computers in the school. The school has no electricity from the national grid, but about 850 school children benefit from this modern facility to learn using new technologies. Information technology (IT) is the key to modern society, and all school children should be exposed to these new technologies

Figure 10.5 The first solar-powered computer system installed in Sri Lanka. Students from SJU had first-hand experience of this new development project during their final-year survey project.

from their early stages of studies. During a survey carried out in September 2008, a team of 85 geography final-year students from Sri Jayawardanepura University (SJU) used this school as part of their studies. The students who participated in this survey came from different parts of the country and were impressed by the way the school buildings were embedded among the indigenous fruit trees such as mangoes and others, producing a cooling effect. The buildings present in the school are not obvious until one walks through the pleasant environment. This kind of project helps young students realise how our future buildings can be built using the coolness of the natural environment without using the power-hungry artificial air-conditioning equipment. Similar systems are now appearing in different parts of the world.

10.7 Applications in Large-Scale Water Pumping (~1,000 W and Above)

This group of students also took part in the opening of the pilot solar village at Kaduruwewa village cluster in Sri Lanka (Fig. 10.6–10.8). They had the opportunity to visit and observe the installed solar-powered water-pumping system which replaced diesel pumps. They also visited a local eco-tourist centre in ‘Ulpotha’ and met the village community during a welcome dinner and an open-air musical evening organised by the villagers. No doubt, these final-year geography students, when graduated and employed, will replicate these socially worthy projects round the country. This needs to happen in every developing country round the globe at large.

University students are our future ambassadors and the backbone of the society for development programmes. Local universities should organise such socially worthy events and projects to provide student experience. Universities, schools, and all organisations should take more social responsibility in nation-building programmes in addition to their mainstream job functions.

This particular solar water-pumping system saves diesel worth Rs. 100,000 (~£600) per annum for the village community. This amount for use of water is deposited by the consumers in a common

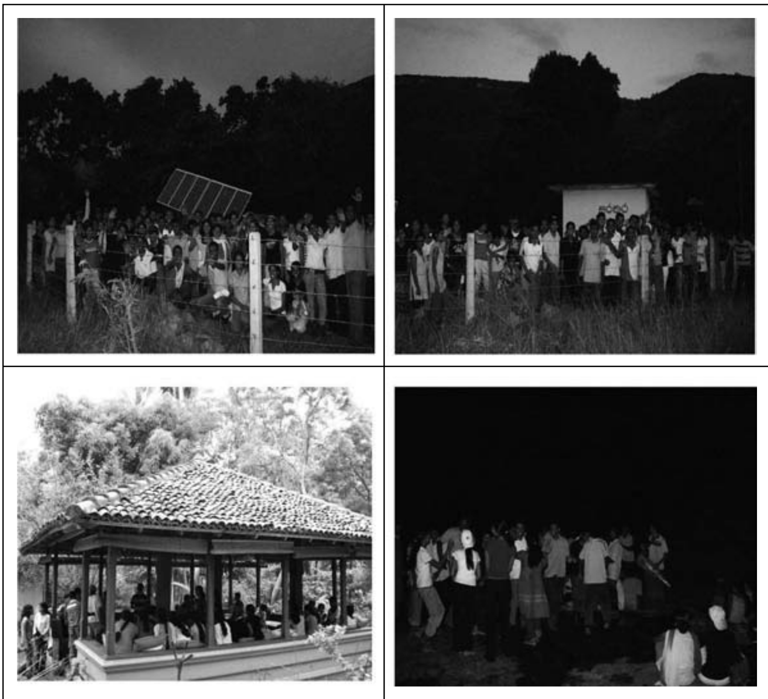

Figure 10.6 Students from SJU experience the solar-powered water-pumping system of the pilot solar village and the nearby eco-tourist centre and enjoy an open-air musical evening organised by the village community.

bank account and managed by the village committee. These funds are used to improve the village kindergarten, primary school, library, and temple and to provide scholarships to bright children in their early stages of education. The author and the team at SJU are guiding the community to manage these funds in an open and transparent way with the highest discipline. This is, in fact, equivalent to establishing a local community banking system and will not be affected by a global banking crisis. They are also encouraging tree planting, organic farming, beekeeping, small industries such as brick making, and other relevant community projects through *sramadana* (voluntary work) to enhance the income to families and the quality of the environment. Explaining scientific facts to village communities in simple terms, how beekeeping can

Figure 10.7 Events during the official opening of the pilot solar village in September 2008 in Sri Lanka.

double or triple their agricultural crops through healthy pollination, motivates everyone to keep several beehives at each home, further contributing to their annual income. These projects empower village communities to develop sustainably, reduce the country's diesel import bill, and help the global community by reducing harmful CO_2 emissions [1, 2].

There are over 3,500 clean-water-pumping systems powered by diesel, and infrastructures have been completed in the dry zone in Sri Lanka. All these diesel pumps can be replaced by solar water-pumping systems and follow the new development projects taking place in the above-mentioned pilot solar village in order to gain all economic and environmental benefits. The replacement of all 3,500 diesel-powered water pumps by solar-powered systems could reduce the diesel import bill by Rs 350 million per annum and the government of Sri Lanka could transfer this amount to our village communities to develop themselves. There are hundreds of

Figure 10.8 A part of the village committee members facing the camera at the solar water-pumping system of the pilot solar village project in Sri Lanka.

agro-wells built in the dry zone, but many of these are unproductive at present due to difficulties in water pumping. All these can be made productive for wealth creation via food production by the installation of solar-powered water-pumping systems. Water-pumping systems can have a wide range of power requirements depending on their size. They can also be expanded as the water demand grows with time. This is a practical example of technology transfer and food production for the modern society.

10.8 Solar Power Applications on Roads

There are many opportunities for the development of our future roads using solar energy. The development of a road network is crucial to the economic development of any country. Road signage, traffic lights, street lighting, and future solar-powered electric car parks are a few examples (Fig. 10.9). Solar-powered street lighting will improve security on roads by removing the need for electric cables and use of electricity from the national grid. In all traffic lights, high-power-consuming filament bulbs should be replaced

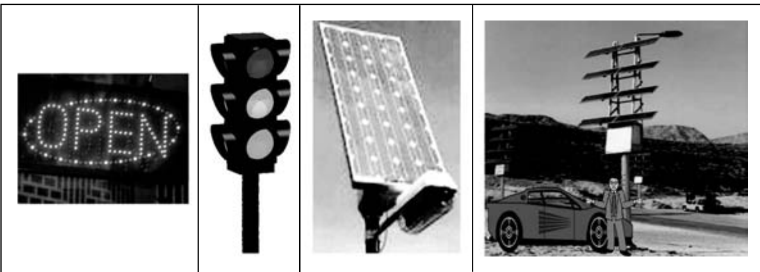

Figure 10.9 Some examples of solar power applications for transport; LED signage, and solar-powered car parks for electric cars. See also Colour Insert.

by low-power LEDs. Then, all traffic lights can be powered by an accompanying solar panel and a battery, ensuring that energy is not used from the national grid and reducing power demand. These systems are already in demand, and the local companies that master these technologies first will have opportunity to win international contracts for such projects from different continents.

Cars with internal combustion engines only will not survive in the future. Manufacturers will move to the production of electric cars via hybrid cars in the transition period. When electric cars are introduced to the society, the battery banks should not be charged from the national grid. The infrastructure should be developed to charge electric cars using renewable energy sources by plugging these into the sun via solar panels or wind turbines. This industry has a huge opportunity for expansion, and the companies that get involve early in this business will experience a fast-moving economic advantage.

10.9 Solar Power Applications on Buildings (∼3 kW and Above)

Solar thermal systems should be installed on every well-developed building in order to provide hot water and, hence, improve washing and health of people. The geysers consuming large amounts of electricity from the national grid should be gradually phased out. Such a policy has been successful in Cyprus with the installation of

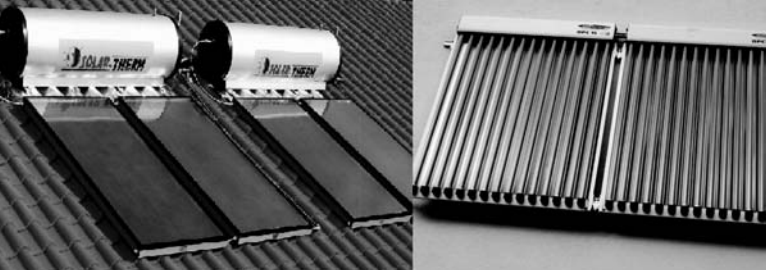

Figure 10.10 Different types of solar thermal systems based on flat plates and vacuum tubes, used to produce hot water for domestic and industrial use. See also Colour Insert.

solar thermal systems on 95% of the buildings. Hotels, hospitals, and care homes are ideal buildings to start these installations. Figure 10.10 shows two different types of solar thermal systems widely used today, and these are comparatively low-tech when compared to PV solar panels.

Building integrated photovoltaics (BIPV) have a huge potential in the future. The advantages of PV are the freely available space on rooftops and walls of existing and new buildings, without the need for any additional land space, and its main feature of not having any moving parts. These small power stations can be connected to the national grid and feed the energy when all the industries are busy working during daytime. Inverters have been designed and manufactured for this purpose. This accessory has been designed to convert DC power into alternating current (AC), step up the voltage, and feed into the grid. Also, the electronic circuitry has been intelligently designed with safety in mind to stop feeding the grid when the grid power is switched off for maintenance purposes. In addition, two-way electric meters (net metering systems) enable a household to import energy from the grid during night-time and export energy into the grid during daytime, using the roof as a small and clean power station. Millions of such solar roofs are now emerging in Japan, the US, Germany, and Italy, reaching grid parity in some places (California and Italy) (Fig. 10.11). All sun-rich countries should learn these new technologies early and apply them in the future.

Figure 10.11 Features of future buildings with PV integrated onto the roofs and walls without occupying any additional land. See also Colour Insert.

In 2004, the cost of a 3 kW solar roof in Germany was about £18,000. However, after eight years, this cost has dropped down to about £9,000. This trend will continue in the future due to improvement of solar panel efficiency, mass production, and the competitiveness of the market place. Regardless, £9,000 for the roof of an average house in Europe costing £250,000 is not an unreasonable amount right now. It has a double purpose, roof for the building and an income source to the household producing clean energy for the future. Since this solar roof cost is still very high for the average family in a developing country, rapid take-up will be slow until costs reduce significantly. However, the production of solar panels locally will reduce this cost by a substantial amount.

Imagine a country like Sri Lanka, with around two million developed homes, having 3 kW solar roofs. During daytime, the power production would be equivalent to 6 GW (Sri Lanka's total power production today is about 3 GW). This should be the long-term strategy of any country in the sun-belt. Also, power generation is not concentrated in one place, reducing the risk from any catastrophe in the future — hence 'PV for Peace'.

Figure 10.12 Solar roofs installed in Sheffield after the introduction of new solar tariff in the United Kingdom in April 2010. See also Colour Insert.

The recommendation for developing countries is to install 'a small number of large systems' in the short term in order to learn and master the technology. Meanwhile, the national grids should be upgraded to a very high standard, minimising transmission losses. Solar roofs can then be introduced on a large scale with confidence, producing energy during daytime.

The policies introduced by governments make a huge difference since the technology is ready for use. A continuing research and development process will gradually bring down the cost. The UK government's introduction of solar tariff of 41.3 pence (£0.41) per unit (kWh) from April 2010 is already showing this effect. Solar roofs producing 2–3 kW power are mushrooming throughout the country. News releases indicate that over 300,000 solar roofs have been installed within the first two years alone during the past two years (Fig. 10.12). These solar roofs are equivalent to about 1 GW power station. Making use of this opportunity, new companies are created to install solar roofs round the country, without any cost to the households. If this becomes a profitable business in the United Kingdom, with low solar insolation, many countries round the globe could do well with the solar roof business. In particular, countries in the sun-belt could thrive with the solar roof business, producing energy from indigenous solar power.

10.10 Energy from Solar Farms and Deserts (MW Range)

Solar energy production is no longer a niche activity. Solar farms are increasing output to 5–10 MW scale and beginning to cover some of the desert areas. Professor Kurokawa's work in the Gobi desert

to produce electricity and cultivate unused lands is a good example. Imagine the desert lands available around the globe; covering the areas of the edge of deserts and connecting these power stations with electric cables could be done easily. The world is not short of energy, but humankind should work to introduce safe energy sources and phase out harmful energy technologies from the society [3, 4]. We have the responsibility to build a safe and peaceful world for our future generations.

10.11 Recommendations for Developing Countries

- Establish a policy to install solar thermal hot water systems on well-developed buildings and gradually phase out electric geysers that consume power from the national grid.
- Rapidly introduce low-power LED lamps to use in solar home systems and other relevant lighting applications in order to reduce power consumption.
- Establish installations of small systems in large numbers. Expand activities on solar home, solar thermal, and small drip irrigation systems to accelerate village electrification and development.
- Establish the installation of large systems in small numbers. Learn the technology rapidly and update the national grid to a high standard, minimising the current level of transmission losses. All renewable applications are complementary and, therefore, relieve the national grid from high power demand.
- Use large community solar water-pumping systems and apply solar village concepts for rapid development. Develop the infrastructure rapidly around the water-pumping systems with all possible support, allowing needy people to stand on their own feet.
- Replace diesel pumps used in already established water-pumping systems using solar water pumps. Install solar water pumps at every suitable source of water and increase food production.

- Establish local community banking system, applying solar village concepts [2], to protect communities from global banking crises.
- Encourage teachers, university dons, clergymen, company employers, and responsible civil servants to be involved in social development projects in addition to their mainstream job functions.
- After the first wave of use of solar energy for agriculture, introduce the second wave of relevant industries. These industries include canning of fresh food and packaging of solar-dried fruits, vegetables and fish. Establish a healthy export business for packaged food products from fertile, green, and lush sun-rich countries.
- Manufacture renewable energy application products using already available and new knowledge created within the country and encourage new inventions through a buoyant research culture.
- Future energy supply will be through hydrogen, produced by the electrolysis of water using freely available energy sources such as solar and wind. Encourage research and development in this direction within each country.
- Encourage tree-planting projects on a large scale in order to re-absorb CO_2 from the atmosphere. This will prevent desertification in some countries and help in water and soil management, the reduction of flash floods and landslides, etc., minimising natural disasters and creating a pleasant environment.

10.12 Recommendations for Developed Countries

- Improve energy efficiency to reduce the consumption of energy per head and reduce CO_2 emissions.
- Establish a policy to install solar thermal hot water systems on every suitable building and gradually phase out electric geysers that consume power from the national grid.

- Rapidly introduce low-power LED lamps in household lighting applications and power these using PV solar panels.
- Encourage teachers, university dons, clergymen, company employers, and responsible civil servants to be involved in social development projects, in addition to their mainstream job functions.
- Future energy supply will be through hydrogen, produced by the electrolysis of water using freely available energy sources such as solar and wind. Encourage research and development in this direction within each country.
- Encourage tree-planting projects on a large scale in order to re-absorb CO_2 from the atmosphere. This will prevent desertification in some countries and help in water and soil management, the reduction of flash floods and landslides, etc., minimising natural disasters and creating a pleasant environment.

10.13 Summary

This chapter described how solar power could assist in the social and economic development of developing and developed countries using various applications at different power levels. The largest impact in developing countries in the short term will come from drip irrigation and community water-pumping systems combined with solar village concepts introduced recently for social development. Solar energy can be used as the first wave of actions to improve agriculture and enhance food production. In the second wave of actions, small industries could be established to benefit from an enhanced food production process and a healthy export business could be developed. Other large-scale solar power applications are also presented, and relevant recommendations are made in order for developing countries to move towards becoming energy-independent and fully developed. The recommendations for developed countries are also presented to help them move towards a low-carbon economy in the future.

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Chapter 11

Is Fermi-Level Pinning Affecting GaAs-Based Solar Cells?

11.1 Introduction

Fermi-level pinning at five discrete levels at metal/n-CdTe interfaces sheds light on new understanding of the CdS/CdTe solar cells. This was made possible purely by the careful observation of experimental results. The appearance of discrete potential barriers and well-defined groups of open circuit voltages are the key observations that led to the new understanding. These results were first published in 2002 for CdS/CdTe solar cells [1], and a similar behaviour for CIGS solar cells was revealed in 2009 [2]. This short chapter briefly examines the experimental results emerging for GaAs-based solar cells to date.

11.2 Observation of Discrete Sets of I-V Characteristics

Experimental results presented in chapters 7, 8, and 9 indicate that solar cell devices or rectifying device structures based on GaAs also show different potential barriers and, hence, different groups

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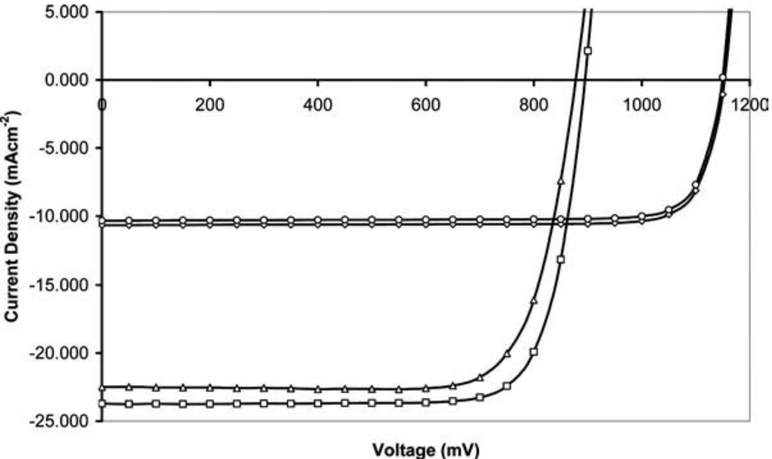

Figure 11.1 Two sets of I-V curves observed for GaAs/AlGaAs-graded bandgap solar cells.

of open circuit voltages. The first growth of GaAs/AlGaAs system provided the highest observed V_{oc} values, in the range 1,145–1,175 mV, for single devices. However, the second growth on a GaAs substrate with a different orientation produced solar cells with V_{oc} values in the range 840–890 mV. These two sets of I-V characteristics shown in Fig. 11.1 clearly indicate the appearance of well-defined and discrete V_{oc} values for GaAs-based solar cells.

11.3 Observation of Discrete Sets of V_{oc} Values

Further observations of relevant publications in the literature show even more striking results. Bauhuis *et al*. [3] carried out similar work in 2007 on GaAs-based solar cells and reported that V_{oc} values appear in two different groups. These values appear in the 840–880 mV or 1005–1045 mV range. Now it is apparent that there exist at least three groups of well-defined V_{oc} values for GaAs devices as summarised in Table 11.1 and this is graphically shown in Fig. 11.2.

Table 11.1 Three groups of open circuit voltages observed for GaAs-based solar cells

Device Type	Open Circuit Voltage Groups Observed (mV)
A	860 ± 20
B	1025 ± 20
C	1160 ± 15

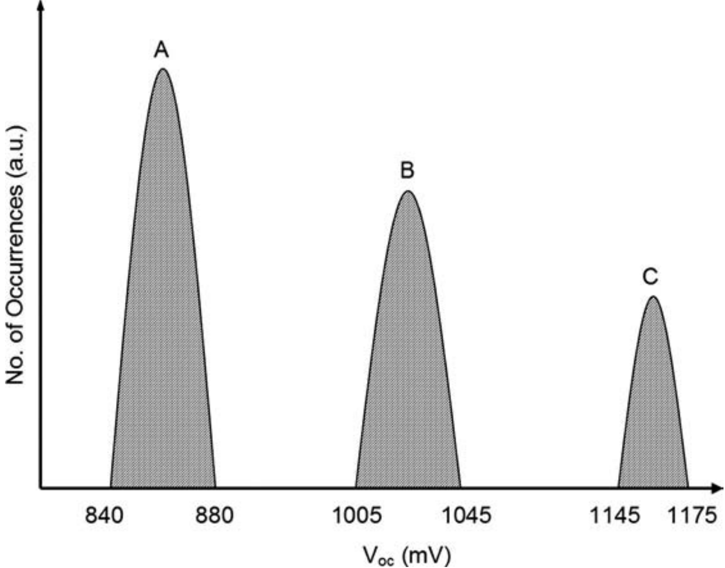

Figure 11.2 A graphical presentation of the three sets of V_{oc} groups observed for GaAs-based solar cells.

11.4 Discussion of New Observations

The effects of defects on solar cell characteristics as discussed in chapter 9 show how defect levels affect GaAs-based solar cells. More comprehensive experimental work or re-examination of already published work may reveal other possible Fermi-level pinning positions for GaAs-based solar cells. However, the results already observed show that the behaviour of GaAs-based solar cells is very

Table 11.2 Experimentally observed defect levels in metal organic vapour phase epitaxy (MOVPE) $Al_xGa_{(1-x)}As$ layers [4, 5]

Al Content (x)	Activation Energy, E_a (eV)	Approximate Concentration (cm^{-3})
0.05–0.11	0.41	10^{14}–10^{16}
0.15	0.50	10^{15}
0.20	0.55	10^{15}
(0.00–0.25)	(0.80–0.90)	The varying EL2 level according to the value of x

similar to those of CdTe- and CIGS-based solar cells. It is appropriate at this stage to refer to the well-researched and documented deep levels in GaAs [4] and AlAs [5] materials in the literature.

There exist a large number of experimentally observed defect levels in MOVPE-grown GaAs and AlAs materials, as summarized in Table 11.2

These observations indicate that the Fermi-level pinning is also affecting GaAs-based solar cells in a way very similar to those observed for CdTe and CIGS-based solar cells. This is the main reason for the observation of open circuit voltages grouped into well-defined clusters.

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Chapter 12

Thoughts on Future Directions of Thin-Film Solar Cell Research and Development

12.1 Introduction

This book presented the advances that took place in thin-film solar cells area, especially during the first decade of the 21st century. All conclusions were made based on experimentally observed results and their scientific interpretations. The main impact is from the understanding of material issues and the underlying physics behind these complex devices. Based on these results and new understanding, this final short chapter presents new areas to focus on, to progress in photovoltaic research and development.

12.2 Areas for Research and Development Efforts

12.2.1 *Dealing with Defects in Thin-Film Device Structures*

As presented in chapters 4, 5, and 11, thin-film solar cells are severely affected by a set of defect levels present in the device

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structure. As the thickness of the semiconducting materials reduces to a few microns and or the sub-micron level in these devices, the surface effects dominate and Fermi-level pinning occurs in all devices based on CdTe, CIGS and GaAs. It is therefore essential to investigate defects in these device structures, eliminate (or passivate) detrimental defects and enhance the helpful defect levels in order to achieve high-efficiency solar cell devices. Otherwise, the presence of numerous defect levels tends to affect the reproducibility, stability, yield and lifetime of thin-film solar cell devices. This area needs urgent attention in order to improve the performance of thin-film solar cell devices.

12.2.2 *Is Impact Ionisation Contributing to the PV Effect?*

This is a very important area to be explored, understood and exploited in PV solar cell devices. In the PV literature, theoretical work has been carried out on impact ionisation [1–4] and quantum efficiency (QE) measurements [5–8]. On several occasions, experimental results exceeding 100% have been reported. Most of these results are not discussed in detail or are not further investigated and exploited in order to improve the PV performance. The latest indications are positive and convincing that impact ionisation takes place in some PV devices [9]. This subject should be thoroughly investigated especially for graded bandgap structures and should be used in PV devices to enhance J_{sc} values.

12.2.3 *Are Intermittent Observations of High* J_{sc} *Values Genuine?*

There are several publications in the literature indicating that the PV conversion efficiencies could reach very high values above 60% [1, 2, 4]. Some theoretical considerations using thermodynamical ideas such as Carnot's principle, indicate maximum achievable efficiencies of above 70% [1, 4, 10]. Unfortunately, innovative ideas in new device design are not forthcoming to practically achieve these high conversion efficiencies.

In the scientific literature, there are many occasions when high J_{sc} values have been experimentally observed and reported, but the PV community has been reluctant to accept these values over the past few decades. On one hand there is a claim that PV efficiencies could reach values over 60% [1, 2, 3], and on the other hand experimentally observed high J_{sc} values exceeding 40 $mAcm^{-2}$, cannot be accepted by the same community. There seems to be a confusion here in the scientific thought process and this needs radical changes in the way we look at and understand the PV process.

At this point it is worth reconsidering the basic expression for the solar energy conversion efficiency given by the following equation:

$$\eta = \frac{V_{oc}.FF.J_{sc}}{P_{in}}$$

In order to achieve high efficiencies, the three parameters, V_{oc}, fill factor (FF), and J_{sc}, should be maximised.

- V_{oc} values are now almost approaching the bandgap of the semiconducting material used. For example, GaAs (E_g = 1.43 eV) produces V_{oc} values of 1.175 V. Therefore V_{oc} values are almost saturating and expected efficiencies above 60% cannot be realised through this parameter.
- FF values have achieved mid-80%, and these are the highest possible values that can be reached for this parameter. Therefore, there is no room for further improvements of conversion efficiency arising from the FF values.
- Then, any anticipated improvements in efficiency must arise from J_{sc}. If we are to double the present-day efficiency, J_{sc} should be doubled. The current average value of J_{sc} ~30 $mAcm^{-2}$ must be doubled to about 60 $mAcm^{-2}$ in order to double our existing efficiencies. It is high time we think differently for the benefit of PV developments

The following is a short communication to the author by a well-respected scientist in the PV field.

14th May 2004

Dear Dr. Dharmadasa

I have read your papers with interest. Giant photocurrents reported by you are a matter of serious Physics. A long time ago when we were working with Cu_2S/CdS *cells, we did observe very high currents even at low efficiencies. Our peers were not very happy with our results and thus we hesitated from publishing such numbers. The good argument is that even if we assume total absorption of all the solar photons and a unit quantum efficiency generating one electron per photon, the photocurrent expected will be no more than half of the highest value you have reported. Yes, graded compositions and thus band gaps do possibly exist though not in any well defined way. But, this cannot explain high currents (since total absorption is already assumed) unless you postulate multi-step absorption processes and multi-electron excitations. If you are serious about your results, you should devise experiments to look into such effects.*

I will draw the attention of our students and colleagues to your results.

Best Wishes

KL Chopra, Professor Emeritus, IITD.

This kind of positive feedback from senior members of the PV community should take place in order to encourage rapid development of this most-needed clean energy production technology. It is clear from this communication that the reluctance to accept high J_{sc} values has been going on during the past four decades hindering rapid PV development. A radical change in thinking is required for the benefit of the PV field!

12.2.4 *Graded Bandgap Multi-Layer Structures for Next-Generation Solar Cells*

The reader's attention is drawn again to the new results presented in chapters 6, 7, and 8 for the positive contribution coming from the

enhanced absorption of a major part of the solar spectrum, multi-electron excitation (or impact ionisation) and multi-step absorption process (or the impurity PV effect) to enhance the performance of PV devices. The graded bandgap multi-layer device design has been experimentally tested using well-researched GaAs-based system. Despite only two growths having been carried out, the highest reported $V_{oc} \approx 1175$ mV with the highest possible FF ≈ 0.86 has been achieved. The short circuit current density values for these initial devices are low in the range 12–24 mAcm^{-2}, due to undesirable doping concentrations in the front and back regions of the device. The highest efficiency achieved from these two growths is $\sim$19% and this value can be increased by optimising the doping concentrations at different regions of this device. These results indicate that the new thought process is in the right direction and future work using low-cost growth techniques to produce this new device structure has a bright future.

The PV effect observed in complete darkness highlights the importance of the new design which is capable of converting the infrared (IR) radiation present in the surroundings to electric power. The combination of the PV power created by sunlight together with the power produced by the surrounding heat radiation will enhance the overall power output of solar panels. This effect should produce high conversion efficiencies exhibiting quantum efficiencies above 100%. The IR radiation available in the surroundings is also coming from our energy source, the sun.

12.3 Conclusions

PV research requires new ways of thinking moving away from traditional thought process. Thin-film solar cells have a very bright future, but the material issues and device physics understanding must be improved in order to achieve high-efficiency and low-cost products. A good part of the scientific research must be devoted to revisiting the existing wisdom from time to time with an open mind and making the required improvements. Otherwise, the errors will propagate through the scientific literature for decades hindering

rapid scientific progress in any field. It has been clearly experienced in the PV research and development field.

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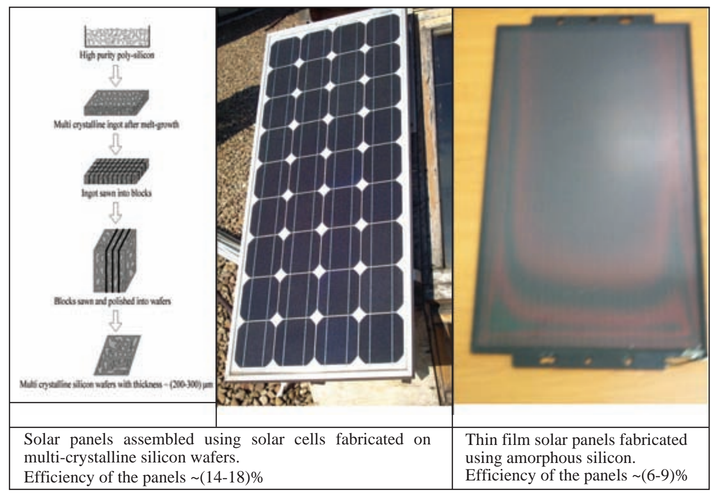

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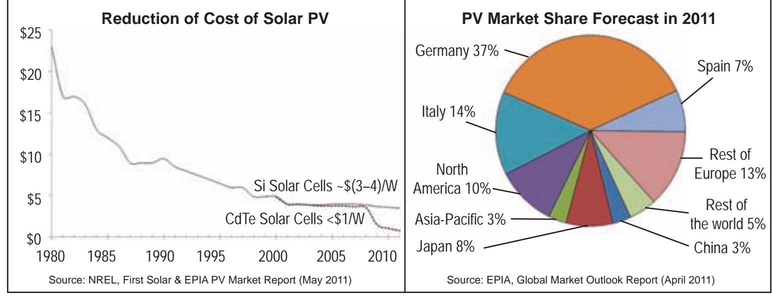

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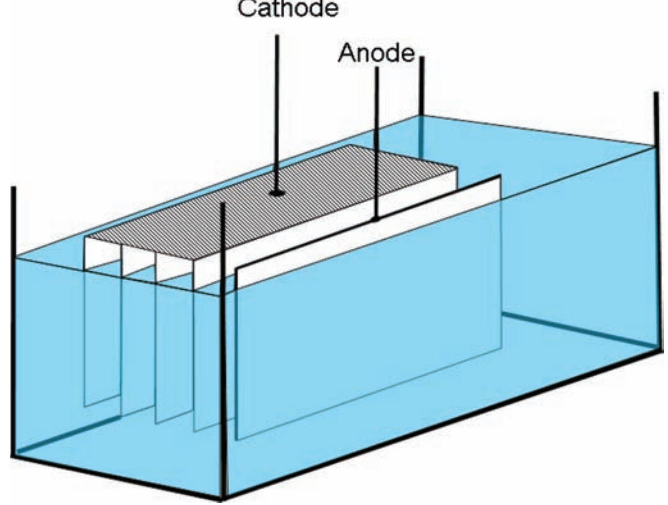

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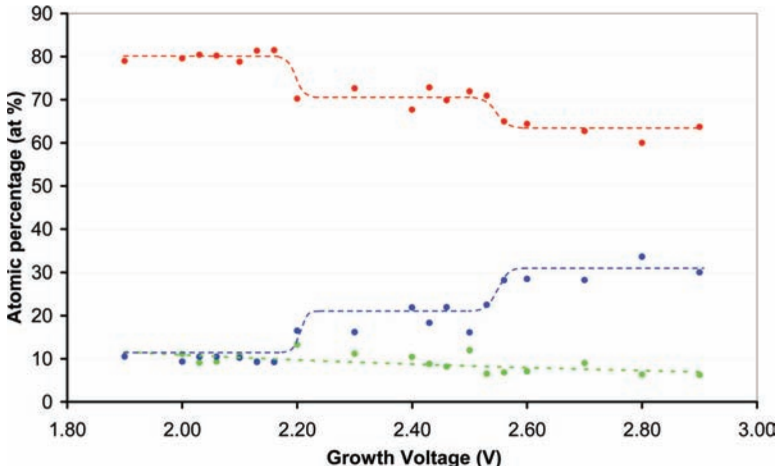

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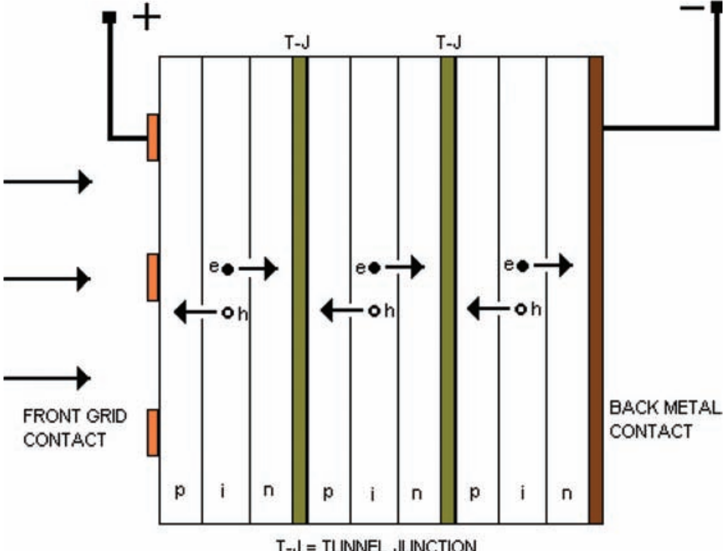

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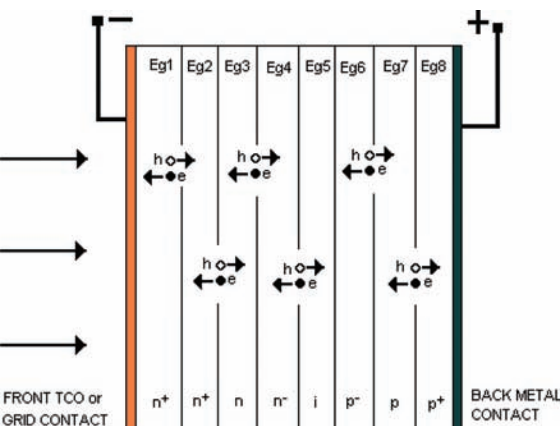

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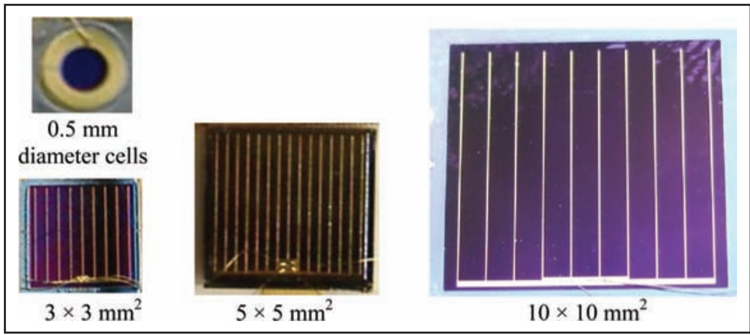

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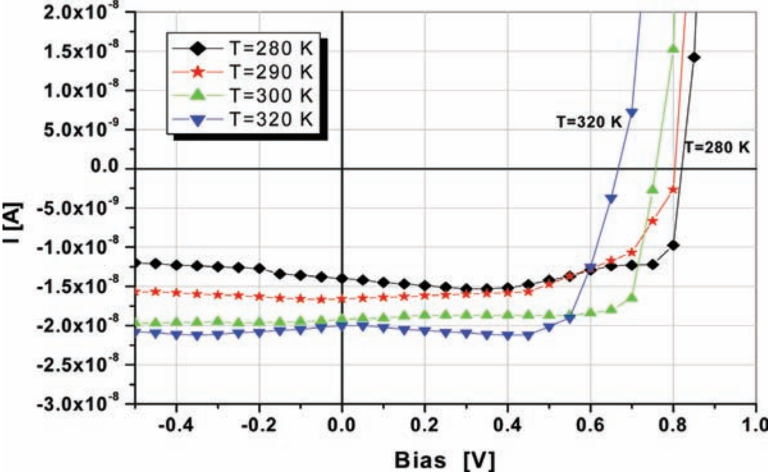

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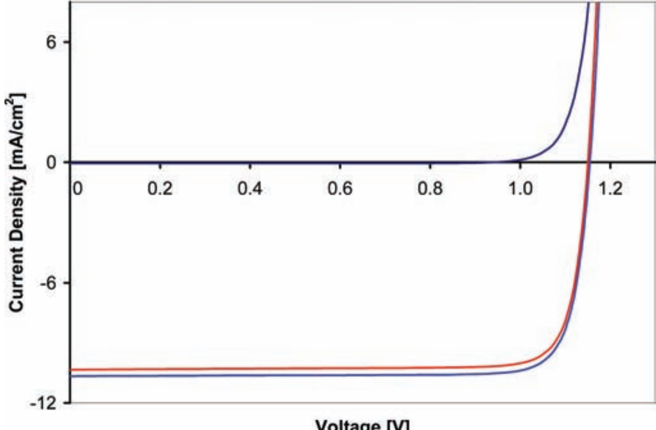

Figure 9.5

Figure 10.1

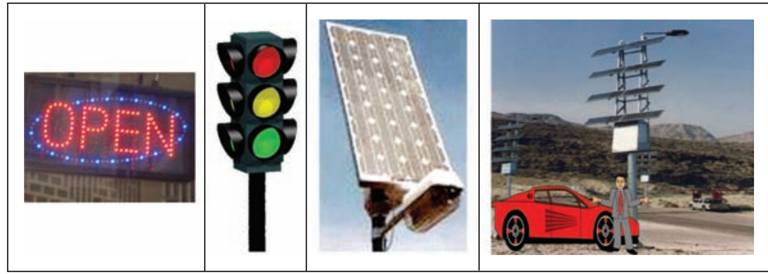

Figure 10.9

Figure 10.10

Figure 10.11

Figure 10.12

Rapid introduction of renewable energy is essential in order to meet future energy demands without further polluting the environment. Solar energy conversion plays a very important role in this, but current solar panels based on silicon are expensive because of the high cost of processing crystalline silicon, a technology that demands high energy consumption. The way forward is to move towards thin-film solar cells using alternative materials and low-cost manufacturing methods. The photovoltaic community is actively researching thin-film solar cells based on amorphous silicon, cadmium telluride (CdTe), copper indium gallium diselenide (CIGS), dye-sensitised materials, and organic semiconductors/polymers. However, progress has been slow owing to the complications of the physics behind these devices.

This book concentrates on the latest developments in and understanding of device physics underlying thin-film solar cells. The material presented is mainly experimental and based on CdTe thin-film solar cells. The author extends these new findings to CIGS- and GaAs-based thin-film solar cells and presents a new device design based on graded bandgap multilayer solar cells. This design has been experimentally tested using the well-researched GaAs/AlGaAs system, and initial devices have shown impressive device parameters ($V_{oc} \approx 1175$ mV, FF ≈ 0.85, and $J_{sc} \approx 12$ mAcm^{-2}). In particular, the V_{oc} represents the highest recorded value together with the highest possible FF values to date for a single PV device, indicating the right approach for PV solar cell development. This device is capable of absorbing all radiation (ultraviolet, visible and infrared) within the solar spectrum as well as heat energy from the surroundings and combines these with "impact ionisation" and "impurity photovoltaic" effects. The conversion efficiency of graded bandgap device has improved to ~20% using only two growth attempts. The improved device understanding presented in this book should impact and guide future device design and low-cost thin-film solar panel development and manufacture.

I. M. Dharmadasa is professor of applied physics and head of the Electronic Materials and Sensors Group at Materials and Engineering Research Institute at Sheffield Hallam University, UK. He has worked extensively in semiconductor research since becoming a PhD student at Durham University as a Commonwealth Scholar, in 1977. He has over 200 publications and presentations on both research and development and applications of solar energy and 6 patents on thin-film solar cells and has successfully supervised 14 PhD programmes to date. Winner of several scholarships and awards, including the 2001 Eurosolar UK Prize for inspiring renewable energy applications, Prof. Dharmadasa is also passionate about promoting the use of renewable energy for economic development and poverty reduction and is active in setting up solar-powered energy hubs in developing countries to empower rural communities through education and commerce. He blogs at www.apsl.org.uk.